XC9500 In-System Programmable CPLD Family

September 15, 1999 (Version 5.0)

Features

- High-performance
  - 5 ns pin-to-pin logic delays on all pins
  - f_{CNT} to 125 MHz
- Large density range
  - 36 to 288 macrocells with 800 to 6,400 usable gates
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3 V or 5 V I/O capability
- Advanced CMOS 5V FastFLASH technology
- Supports parallel programming of multiple XC9500 devices

Family Overview

The XC9500 CPLD family provides advanced in-system programming and test capabilities for high performance, general purpose logic integration. All devices are in-system programmable for a minimum of 10,000 program/erase cycles. Extensive IEEE 1149.1 (JTAG) boundary-scan support is also included on all family members.

As shown in Table 1, logic density of the XC9500 devices ranges from 800 to over 6,400 usable gates with 36 to 288 registers, respectively. Multiple package options and associated I/O capacity are shown in Table 2. The XC9500 family is fully pin-compatible allowing easy design migration across multiple density options in a given package footprint.

The XC9500 architectural features address the requirements of in-system programmability. Enhanced pin-locking capability avoids costly board rework. An expanded JTAG instruction set allows version control of programming patterns and in-system debugging. In-system programming throughout the full device operating range and a minimum of 10,000 program/erase cycles provide worry-free reconfigurations and system field upgrades.

Advanced system features include output slew rate control and user-programmable ground pins to help reduce system noise. I/Os may be configured for 3.3 V or 5 V operation. All outputs provide 24 mA drive.

Architecture Description

Each XC9500 device is a subsystem consisting of multiple Function Blocks (FBs) and I/O Blocks (IOBs) fully interconnected by the FastCONNECT switch matrix. The IOB provides buffering for device inputs and outputs. Each FB provides programmable logic capability with 36 inputs and 18 outputs. The FastCONNECT switch matrix connects all FB outputs and input signals to the FB inputs. For each FB, 12 to 18 outputs (depending on package pin-count) and associated output enable signals drive directly to the IOBs. See Figure 1.

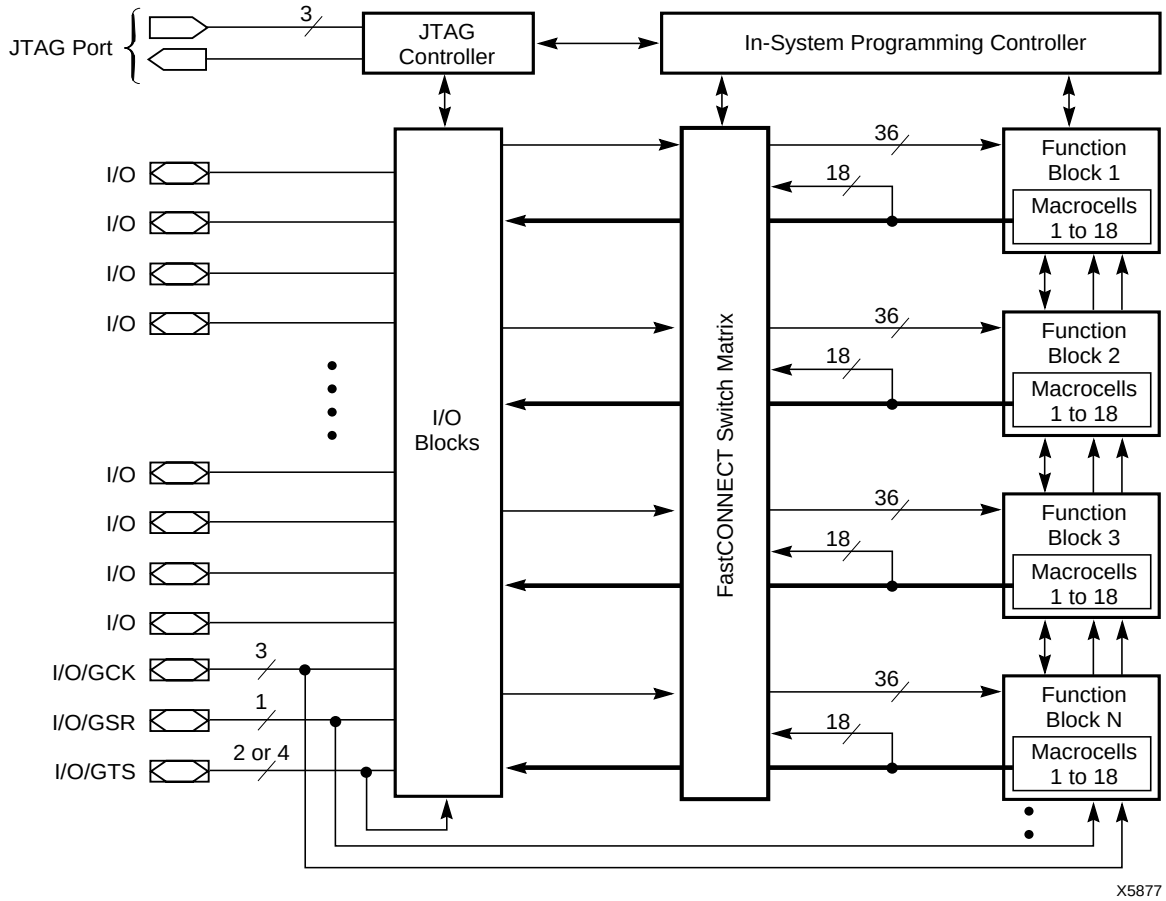

Figure 1: XC9500 Architecture

Note: Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

Table 1: XC9500 Device Family

	XC9536	XC9572	XC95108	XC95144	XC95216	XC95288
Macrocells	36	72	108	144	216	288
Usable Gates	800	1,600	2,400	3,200	4,800	6,400
Registers	36	72	108	144	216	288
t_{PD} (ns)	5	7.5	7.5	7.5	10	10
t_{SU} (ns)	3.5	4.5	4.5	4.5	6.0	6.0
t_{CO} (ns)	4.0	4.5	4.5	4.5	6.0	6.0
f_{CNT} (MHz)	100	125	125	125	111.1	111.1
f_{SYSTEM} (MHz)	100	83.3	83.3	83.3	66.7	66.7

Note: f_{CNT} = Operating frequency for 16-bit counters
f_{SYSTEM} = Internal operating frequency for general purpose system designs spanning multiple FBs.

Table 2: Available Packages and Device I/O Pins (not including dedicated JTAG pins)

	XC9536	XC9572	XC95108	XC95144	XC95216	XC95288
44-Pin VQFP	34					
44-Pin PLCC	34	34				
48-Pin CSP	34					
84-Pin PLCC		69	69			
100-Pin TQFP		72	81	81		
100-Pin PQFP		72	81	81		
160-Pin PQFP			108	133	133	
208-Pin HQFP					166	168
352-Pin BGA					166	192

Function Block

Each Function Block, as shown in Figure 2, is comprised of 18 independent macrocells, each capable of implementing a combinatorial or registered function. The FB also receives global clock, output enable, and set/reset signals. The FB generates 18 outputs that drive the FastCONNECT switch matrix. These 18 outputs and their corresponding output enable signals also drive the IOB.

Logic within the FB is implemented using a sum-of-products representation. Thirty-six inputs provide 72 true and complement signals into the programmable AND-array to form 90 product terms. Any number of these product terms, up to the 90 available, can be allocated to each macrocell by the product term allocator.

Each FB (except for the XC9536) supports local feedback paths that allow any number of FB outputs to drive into its own programmable AND-array without going outside the FB. These paths are used for creating very fast counters and state machines where all state registers are within the same FB.

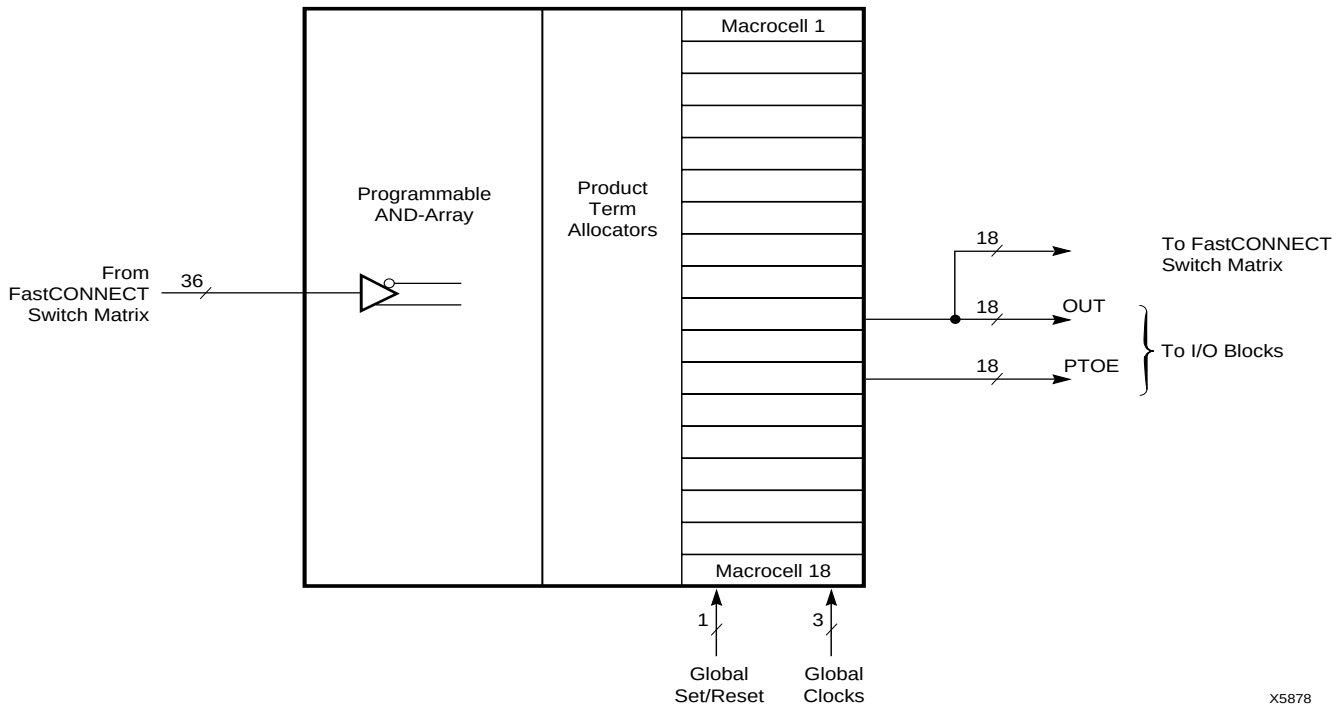

Figure 2: XC9500 Function Block

Macrocell

Each XC9500 macrocell may be individually configured for a combinatorial or registered function. The macrocell and associated FB logic is shown in Figure 3.

Five direct product terms from the AND-array are available for use as primary data inputs (to the OR and XOR gates) to implement combinatorial functions, or as control inputs including clock, set/reset, and output enable. The product term allocator associated with each macrocell selects how the five direct terms are used.

The macrocell register can be configured as a D-type or T-type flip-flop, or it may be bypassed for combinatorial operation. Each register supports both asynchronous set and reset operations. During power-up, all user registers are initialized to the user-defined preload state (default to 0 if unspecified).

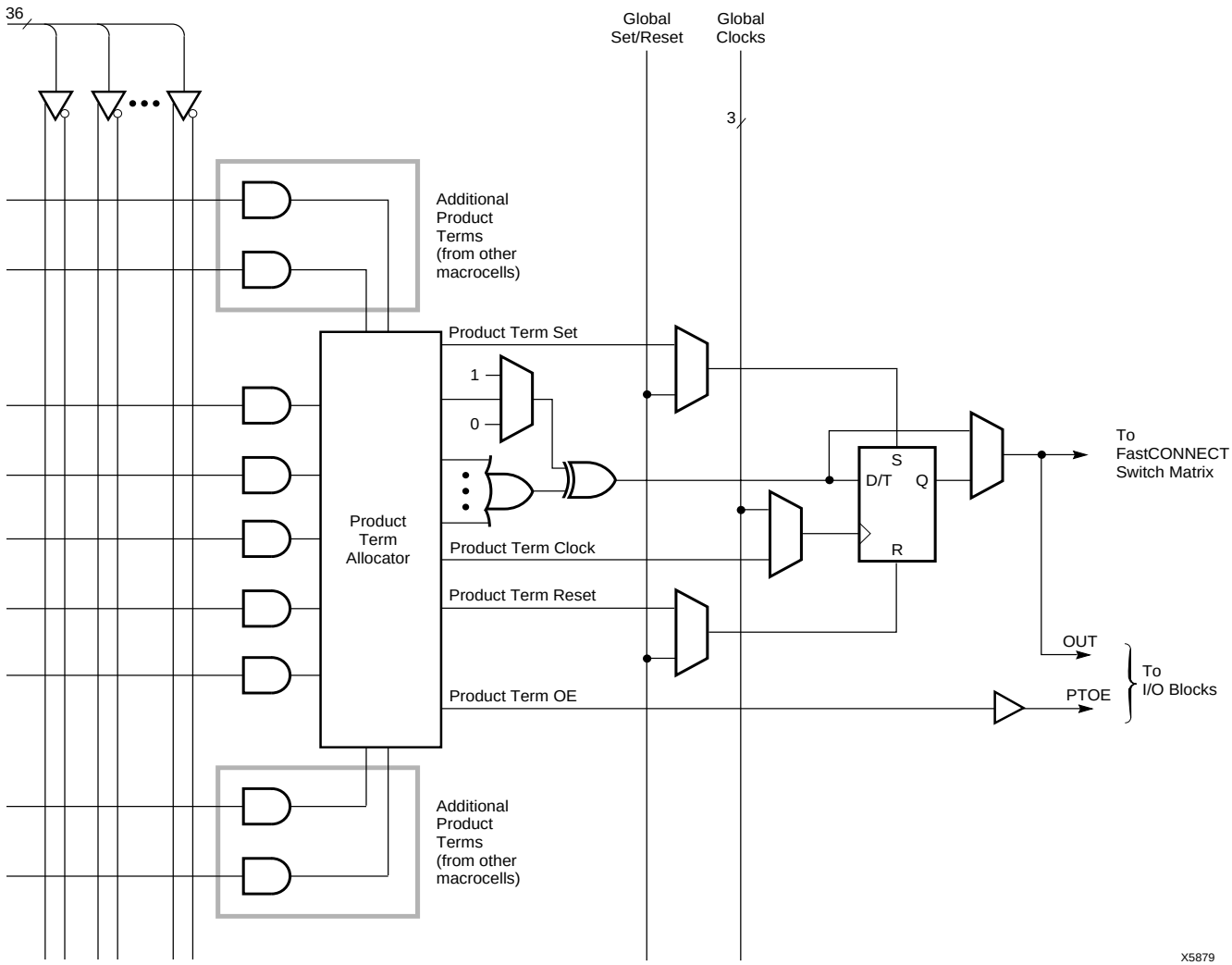

Figure 3: XC9500 Marcocell Within Function Block

All global control signals are available to each individual macrocell, including clock, set/reset, and output enable signals. As shown in Figure 4, the macrocell register clock originates from either of three global clocks or a product term clock. Both true and complement polarities of a GCK pin can be used within the device. A GSR input is also provided to allow user registers to be set to a user-defined state.

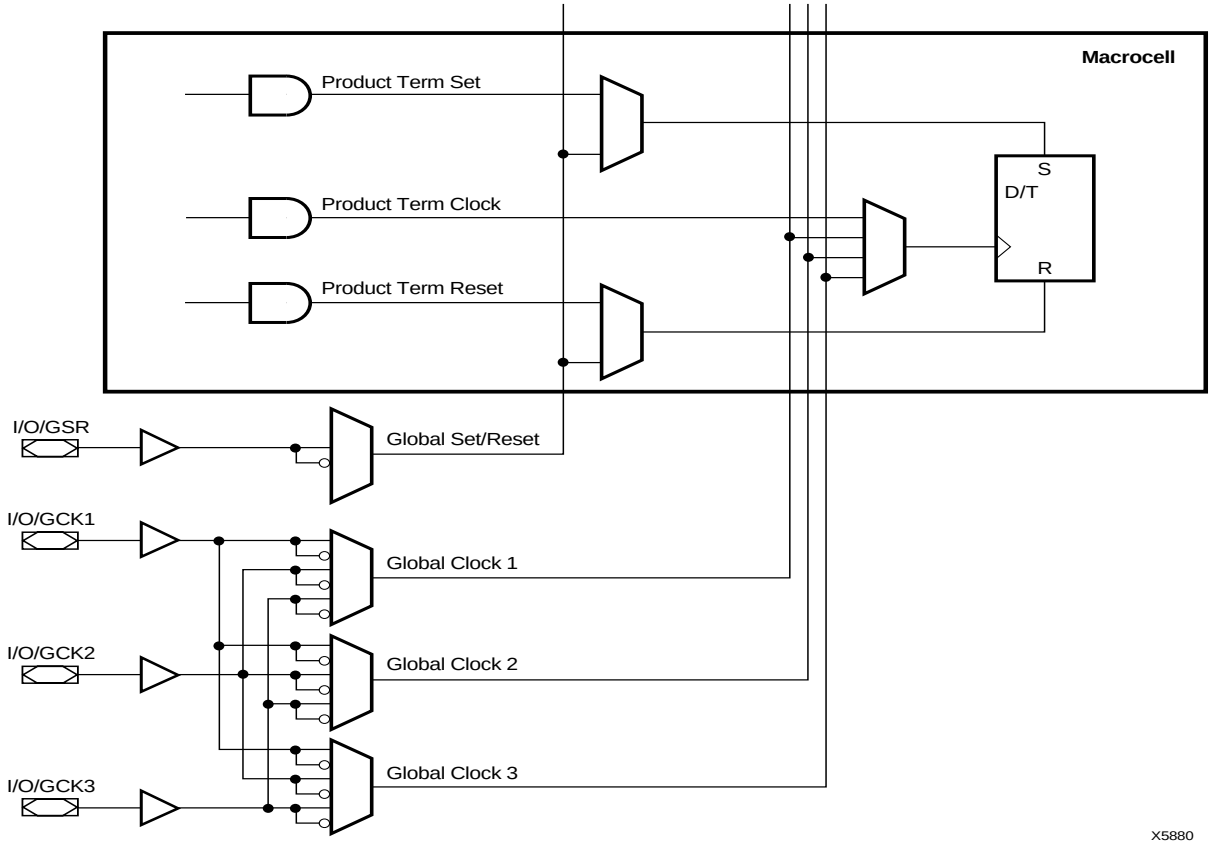

Figure 4: Macrocell Clock and Set/Reset Capability

Product Term Allocator

The product term allocator controls how the five direct product terms are assigned to each macrocell. For example, all five direct terms can drive the OR function as shown in Figure 5.

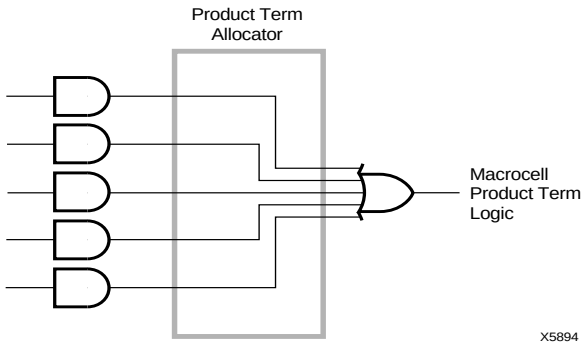

Figure 5: Macrocell Logic Using Direct Product Term

The product term allocator can re-assign other product terms within the FB to increase the logic capacity of a macrocell beyond five direct terms. Any macrocell requiring additional product terms can access uncommitted product terms in other macrocells within the FB. Up to 15 product terms can be available to a single macrocell with only a small incremental delay of $t_{PTA,}$ as shown in Figure 6.

Note that the incremental delay affects only the product terms in other macrocells. The timing of the direct product terms is not changed.

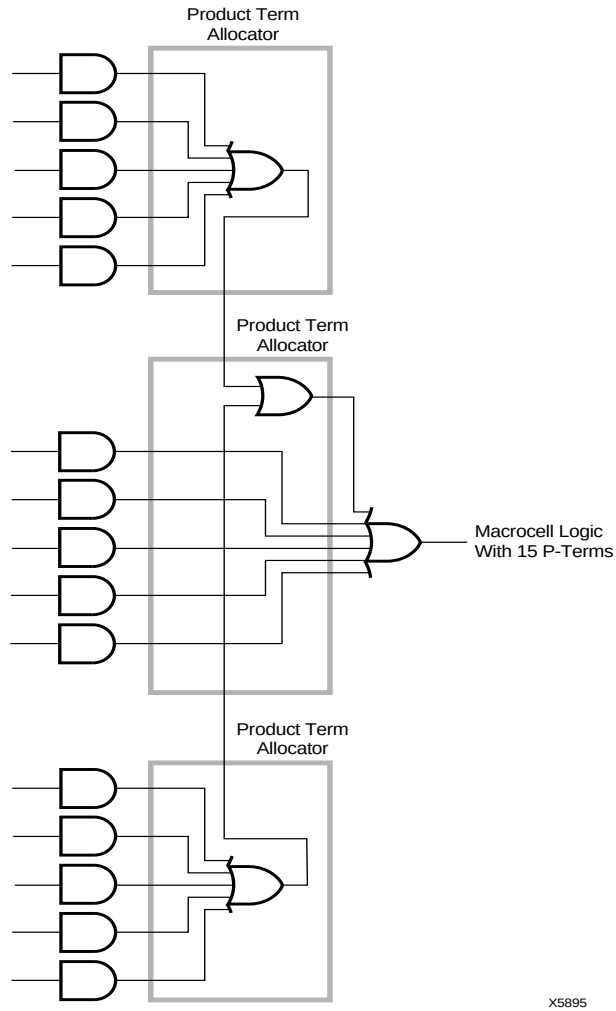

Figure 6: Product Term Allocation With 15 Product Terms

The product term allocator can re-assign product terms from any macrocell within the FB by combining partial sums of products over several macrocells, as shown in Figure 7.

In this example, the incremental delay is only $2*t_{PTA}$. All 90 product terms are available to any macrocell, with a maximum incremental delay of $8*t_{PTA}$.

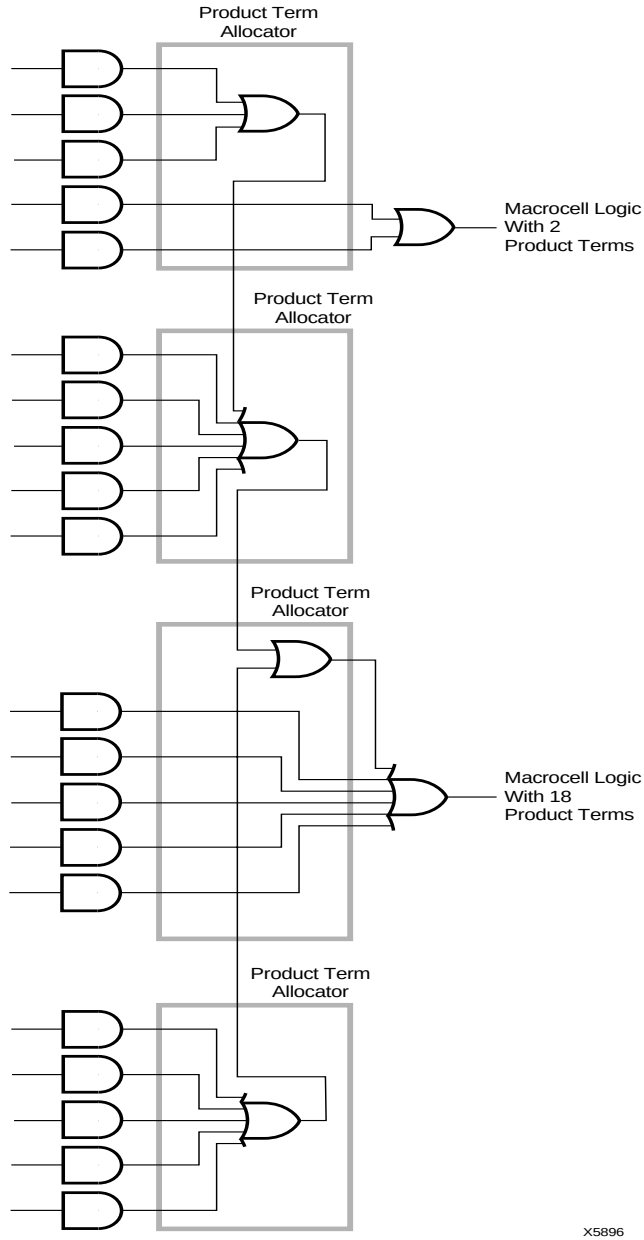

Figure 7: Product Term Allocation Over Several Macrocells

The internal logic of the product term allocator is shown in Figure 8.

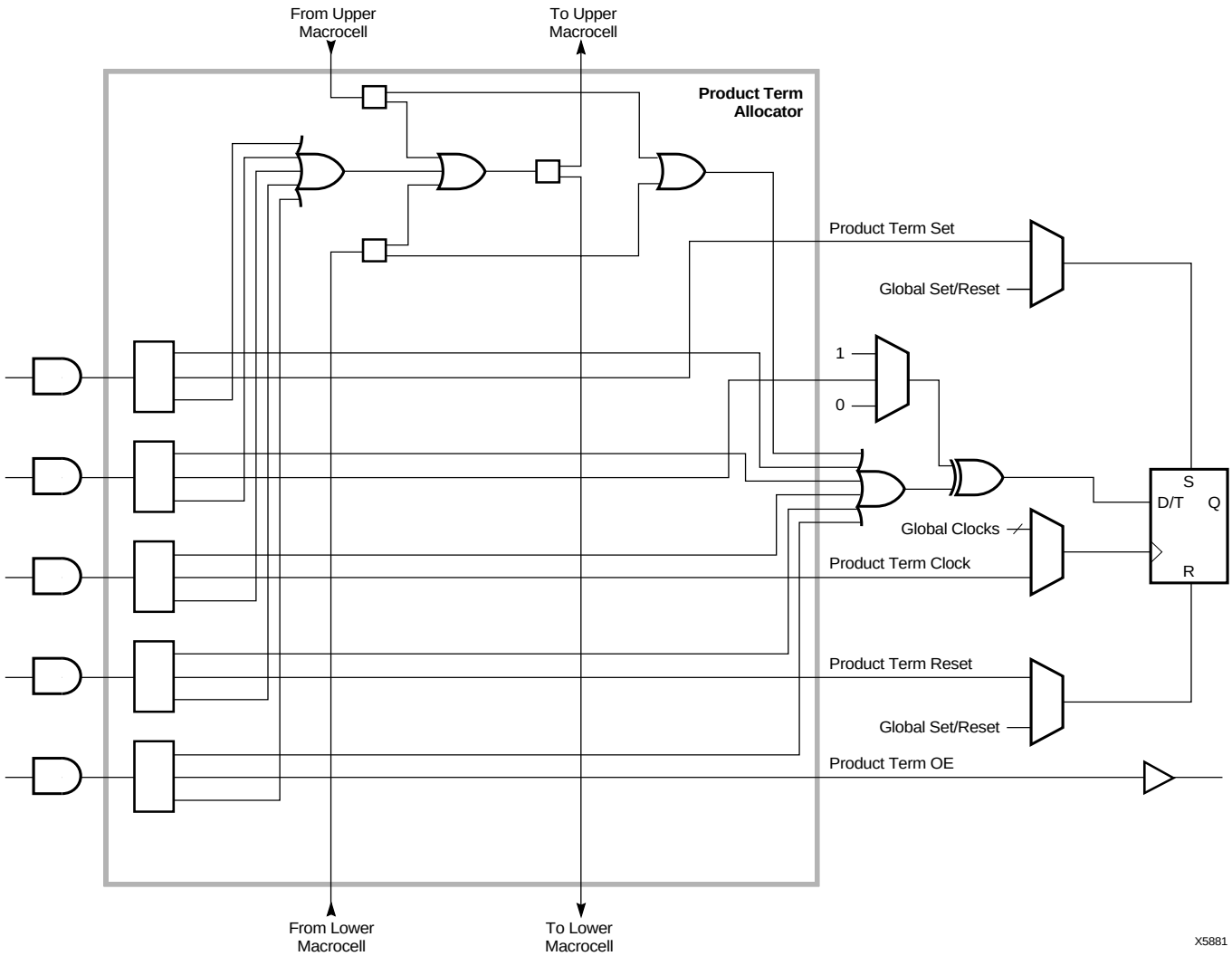

Figure 8: Product Term Allocator Logic

FastCONNECT Switch Matrix

The FastCONNECT switch matrix connects signals to the FB inputs, as shown in Figure 9. All IOB outputs (corresponding to user pin inputs) and all FB outputs drive the FastCONNECT matrix. Any of these (up to a FB fan-in limit of 36) may be selected, through user programming, to drive each FB with a uniform delay.

The FastCONNECT switch matrix is capable of combining multiple internal connections into a single wired-AND output before driving the destination FB. This provides additional logic capability and increases the effective logic fan-in of the destination FB without any additional timing delay. This capability is available for internal connections originating from FB outputs only. It is automatically invoked by the development software where applicable.

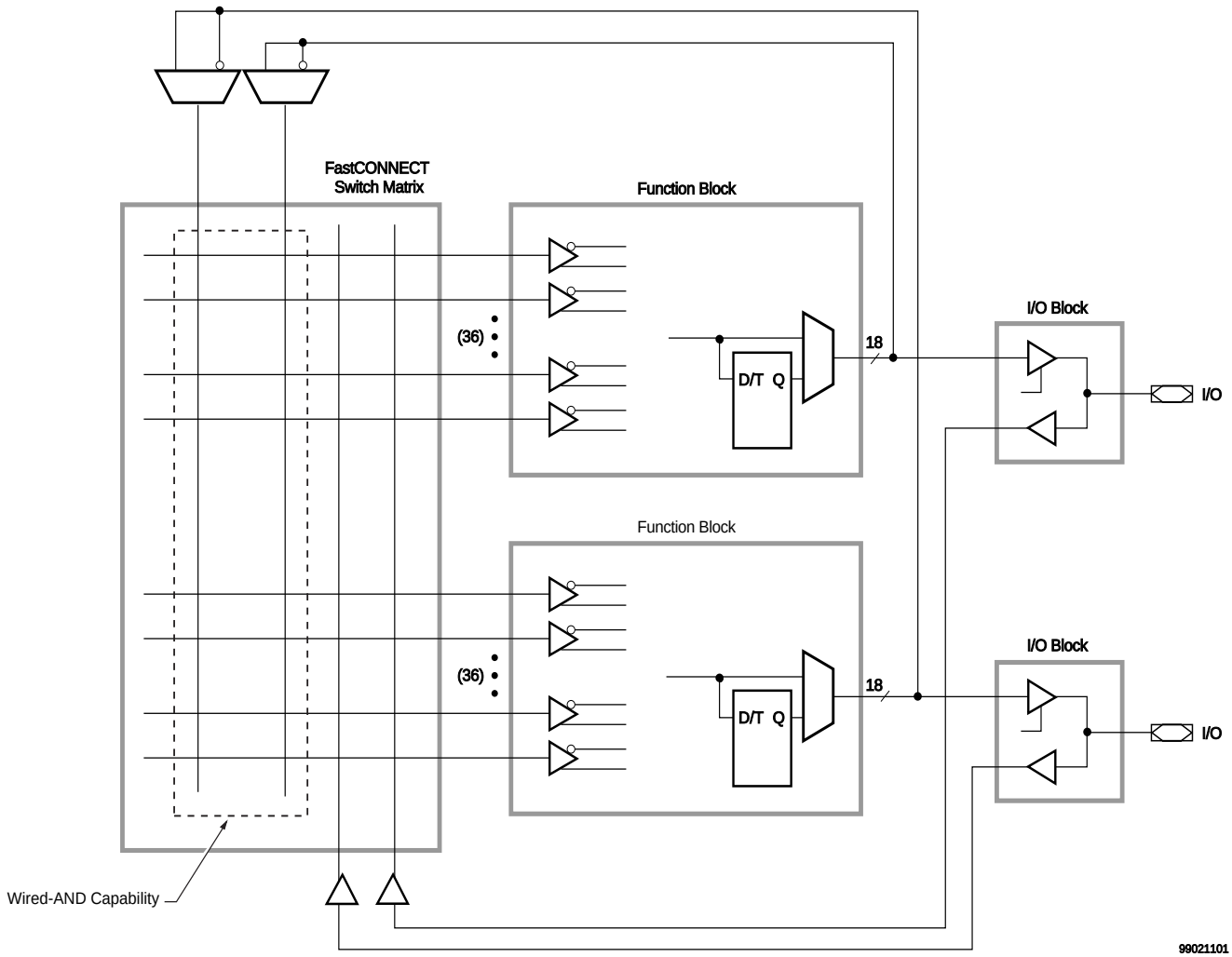

Figure 9: FastCONNECT Switch Matrix

I/O Block

The I/O Block (IOB) interfaces between the internal logic and the device user I/O pins. Each IOB includes an input buffer, output driver, output enable selection multiplexer, and user programmable ground control. See Figure 10 for details.

The input buffer is compatible with standard 5 V CMOS, 5 V TTL and 3.3 V signal levels. The input buffer uses the internal 5 V voltage supply (V_{CCINT}) to ensure that the input thresholds are constant and do not vary with the V_{CCIO} voltage.

The output enable may be generated from one of four options: a product term signal from the macrocell, any of the global OE signals, always “1”, or always “0”. There are two global output enables for devices with up to 144 macrocells, and four global output enables for devices with 180 or more macrocells. Both polarities of any of the global 3-state control (GTS) pins may be used within the device.

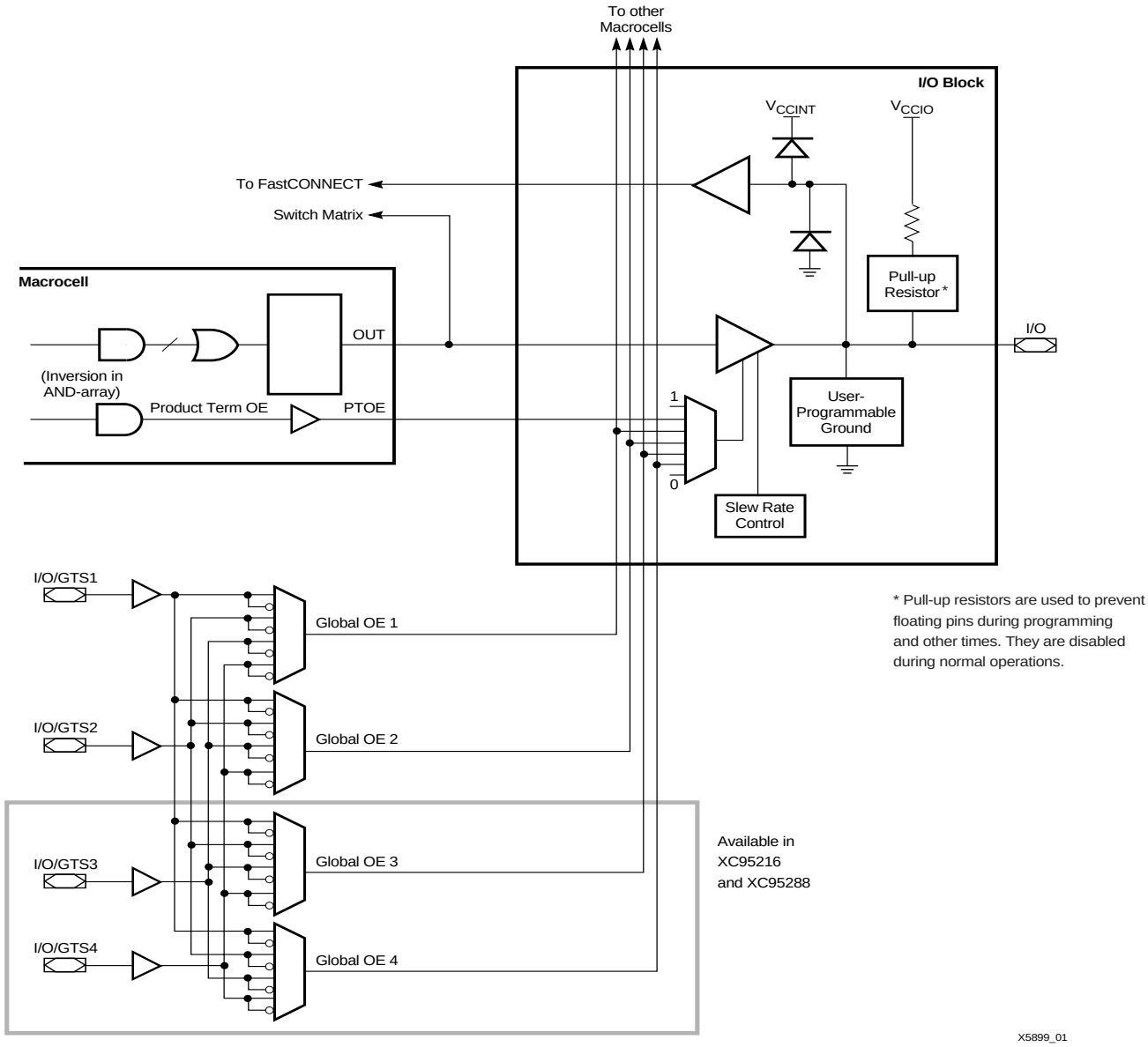

Figure 10: I/O Block and Output Enable Capability

Each output has independent slew rate control. Output edge rates may be slowed down to reduce system noise (with an additional time delay of t_{SLEW}) through programming. See Figure 11.

Each IOB provides user programmable ground pin capability. This allows device I/O pins to be configured as additional ground pins. By tying strategically located programmable ground pins to the external ground connection, system noise generated from large numbers of simultaneous switching outputs may be reduced.

A control pull-up resistor (typically 10K ohms) is attached to each device I/O pin to prevent them from floating when the device is not in normal user operation. This resistor is active during device programming mode and system power-up. It is also activated for an erased device. The resistor is deactivated during normal operation.

The output driver is capable of supplying 24 mA output drive. All output drivers in the device may be configured for either 5 V TTL levels or 3.3 V levels by connecting the device output voltage supply (V_{CCIO}) to a 5 V or 3.3 V voltage supply. Figure 12 shows how the XC9500 device can be used in 5 V only and mixed 3.3 V/5 V systems.

Pin-Locking Capability

The capability to lock the user defined pin assignments during design changes depends on the ability of the architecture to adapt to unexpected changes. The XC9500 devices have architectural features that enhance the ability to accept design changes while maintaining the same pinout.

The XC9500 architecture provides maximum routing within the FastCONNECT switch matrix, and incorporates a flexible Function Block that allows block-wide allocation of available product terms. This provides a high level of confidence of maintaining both input and output pin assignments for unexpected design changes.

For extensive design changes requiring higher logic capacity than is available in the initially chosen device, the new design may be able to fit into a larger pin-compatible device using the same pin assignments. The same board may be used with a higher density device without the expense of board rework.

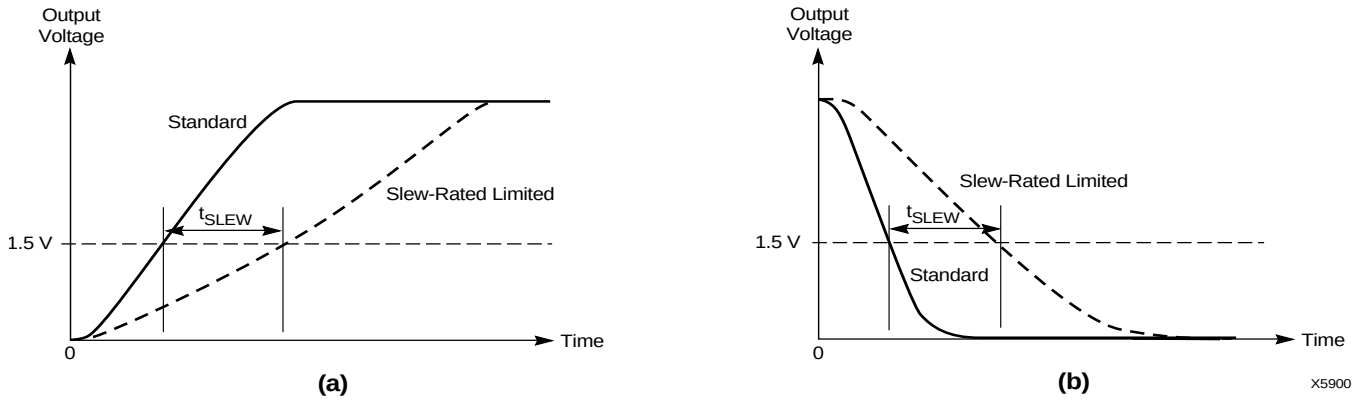

Figure 11: Output Slew-Rate For (a) Rising and (b) Falling Outputs

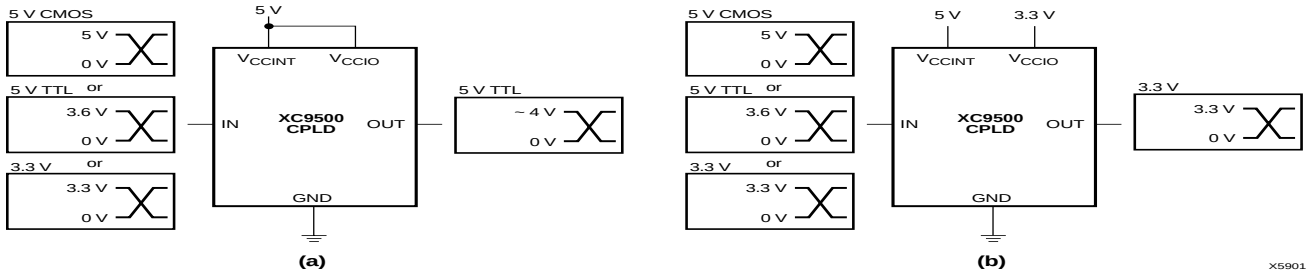

Figure 12: XC9500 Devices in (a) 5 V Systems and (b) Mixed 3.3 V/5 V Systems

In-System Programming

XC9500 devices are programmed in-system via a standard 4-pin JTAG protocol, as shown in Figure 13. In-system programming offers quick and efficient design iterations and eliminates package handling. The Xilinx development system provides the programming data sequence using a Xilinx download cable, a third-party JTAG development system, JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence.

All I/Os are 3-stated and pulled high by the IOB resistors during in-system programming. If a particular signal must remain low during this time, then a pulldown resistor may be added to the pin.

External Programming

XC9500 devices can also be programmed by the Xilinx HW130 device programmer as well as third-party programmers. This provides the added flexibility of using pre-programmed devices during manufacturing, with an in-system programmable option for future enhancements.

Endurance

All XC9500 CPLDs provide a minimum endurance level of 10,000 in-system program/erase cycles. Each device meets all functional, performance, and data retention specifications within this endurance limit.

IEEE 1149.1 Boundary-Scan (JTAG)

XC9500 devices fully support IEEE 1149.1 boundary-scan (JTAG). EXTEST, SAMPLE/PRELOAD, BYPASS, USERCODE, INTEST, IDCODE, and HIGHZ instructions are supported in each device. For ISP operations, five additional instructions are added; the ISPEN, FERASE, FPGM, FVFY, and ISPEX instructions are fully compliant extensions of the 1149.1 instruction set.

The TMS and TCK pins have dedicated pull-up resistors as specified by the IEEE 1149.1 standard.

Boundary Scan Description Language (BSDL) files for the XC9500 are included in the development system and are available on the Xilinx FTP site.

Design Security

XC9500 devices incorporate advanced data security features which fully protect the programming data against unauthorized reading or inadvertent device erasure/reprogramming. Table 3 shows the four different security settings available.

The read security bits can be set by the user to prevent the internal programming pattern from being read or copied. When set, they also inhibit further program operations but allow device erase. Erasing the entire device is the only way to reset the read security bit.

The write security bits provide added protection against accidental device erasure or reprogramming when the JTAG pins are subject to noise, such as during system power-up. Once set, the write-protection may be deactivated when the device needs to be reprogrammed with a valid pattern.

Table 3: Data Security Options

		Read Security: Default	Read Security: Set
Write Security	Default	Read Allowed Program/Erase Allowed	Read Inhibited Program Inhibited/Erase Allowed
	Set	Read Allowed Program/Erase Inhibited	Read Inhibited Program/Erase Inhibited

X5905

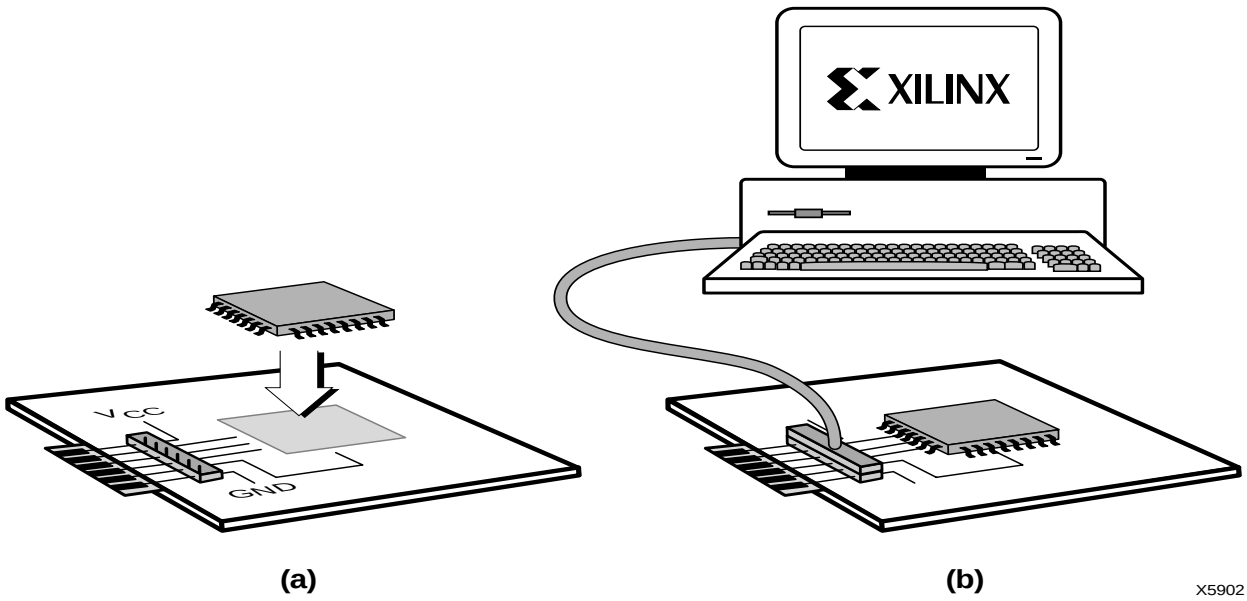

Figure 13: In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable

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Low Power Mode

All XC9500 devices offer a low-power mode for individual macrocells or across all macrocells. This feature allows the device power to be significantly reduced.

Each individual macrocell may be programmed in low-power mode by the user. Performance-critical parts of the application can remain in standard power mode, while other parts of the application may be programmed for low-power operation to reduce the overall power dissipation. Macrocells programmed for low-power mode incur additional delay (t_{LP}) in pin-to-pin combinatorial delay as well as register setup time. Product term clock to output and product term output enable delays are unaffected by the macrocell power-setting.

Timing Model

The uniformity of the XC9500 architecture allows a simplified timing model for the entire device. The basic timing model, shown in Figure 14, is valid for macrocell functions that use the direct product terms only, with standard power setting, and standard slew rate setting. Table 4 shows how each of the key timing parameters is affected by the product term allocator (if needed), low-power setting, and slew-limited setting.

The product term allocation time depends on the logic span of the macrocell function, which is defined as one less than the maximum number of allocators in the product term path. If only direct product terms are used, then the logic span is 0. The example in Figure 6 shows that up to 15 product terms are available with a span of 1. In the case of Figure 7, the 18 product term function has a span of 2.

Detailed timing information may be derived from the full timing model shown in Figure 15. The values and explanations for each parameter are given in the individual device data sheets.

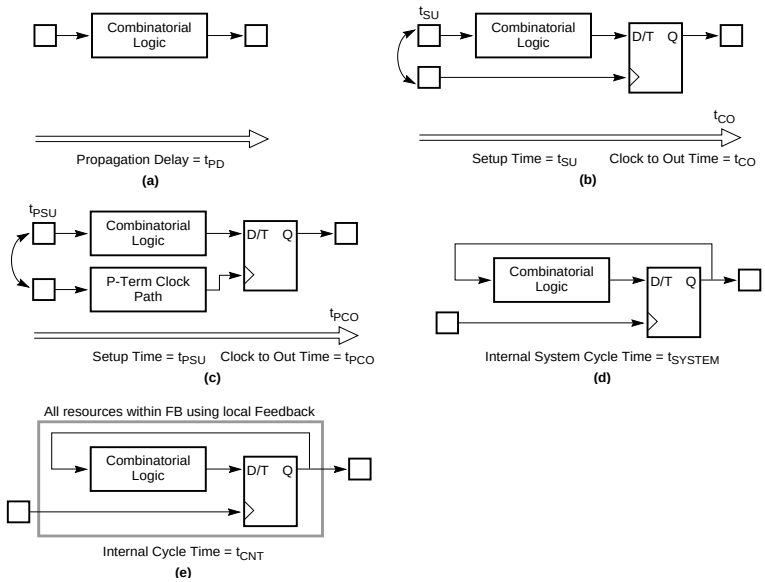

Figure 14: Basic Timing Model

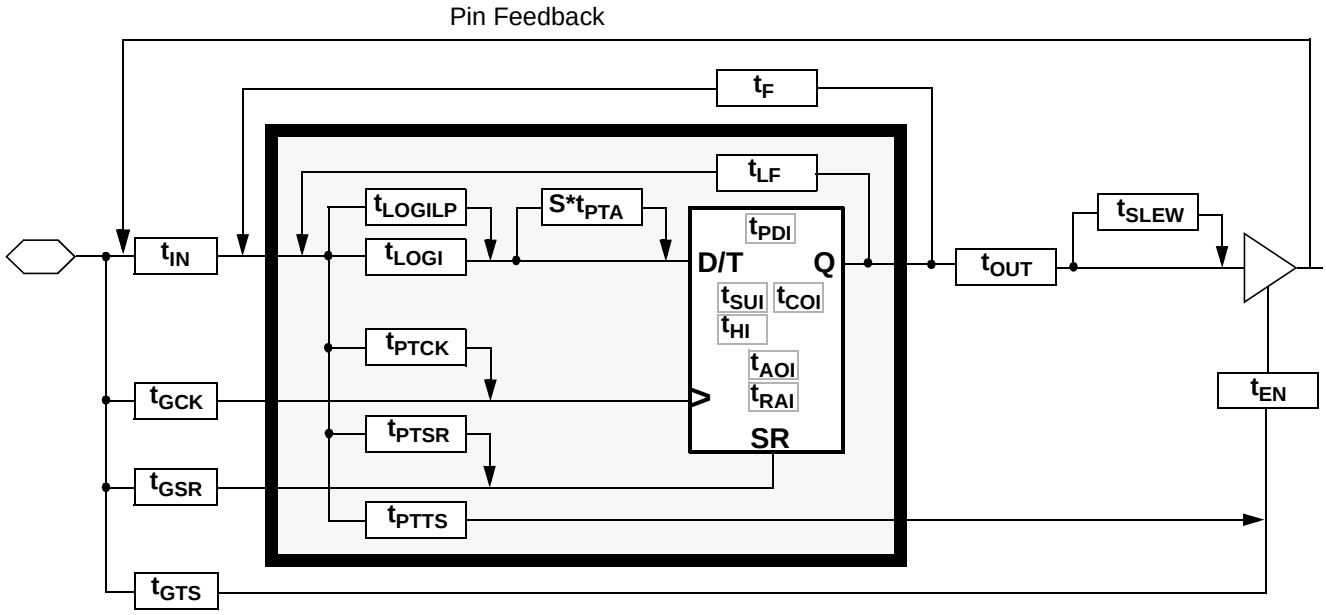

Figure 15: Detailed Timing Model

Power-Up Characteristics

The XC9500 devices are well behaved under all operating conditions. During power-up each XC9500 device employs internal circuitry which keeps the device in the quiescent state until the V_{CCINT} supply voltage is at a safe level (approximately 3.8 V). During this time, all device pins and JTAG pins are disabled and all device outputs are disabled with the IOB pull-up resistors (~ 10K ohms) enabled, as shown in Table 5. When the supply voltage reaches a safe level, all user registers become initialized (typically within 100 µs for 9536 - 95144, 200 µs for 95216 and 300 µs for 95288), and the device is immediately available for operation, as shown in Figure 16.

If the device is in the erased state (before any user pattern is programmed), the device outputs remain disabled with the IOB pull-up resistors enabled. The JTAG pins are enabled to allow the device to be programmed at any time.

If the device is programmed, the device inputs and outputs take on their configured states for normal operation. The JTAG pins are enabled to allow device erasure or boundary-scan tests at any time.

Development System Support

The XC9500 CPLD family is fully supported by the development systems available from Xilinx and the Xilinx Alliance Program vendors.

The designer can create the design using ABEL, schematics, equations, VHDL, or Verilog in a variety of software front-end tools. The development system can be used to implement the design and generate a JEDEC bitmap which can be used to program the XC9500 device. Each development system includes JTAG download software that can be used to program the devices via the standard JTAG interface and a download cable.

FastFLASH Technology

An advanced CMOS Flash process is used to fabricate all XC9500 devices. Specifically developed for Xilinx in-system programmable CPLDs, the FastFLASH process provides high performance logic capability, fast programming times, and endurance of 10,000 program/erase cycles.

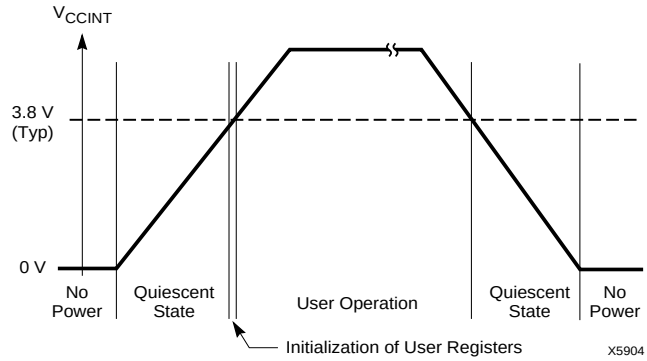

Figure 16: Device Behavior During Power-up

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Table 4: Timing Model Parameters

Description	Parameter	Product Term Allocator[1]	Macrocell Low-Power Setting	Output Slew-Limited Setting
Propagation Delay	t_{PD}	+ t_{PTA} * S	+ t_{LP}	+ t_{SLEW}
Global Clock Setup Time	t_{SU}	+ t_{PTA} * S	+ t_{LP}	–
Global Clock-to-output	t_{CO}	–	–	+ t_{SLEW}
Product Term Clock Setup Time	t_{PSU}	+ t_{PTA} * S	+ t_{LP}	–
Product Term Clock-to-output	t_{PCO}	–	–	+ t_{SLEW}
Internal System Cycle Period	t_{SYSTEM}	+ t_{PTA} * S	+ t_{LP}	–

Note: 1. S = the logic span of the function, as defined in the text.

Table 5: XC9500 Device Characteristics

Device Circuitry	Quiescent State	Erased Device Operation	Valid User Operation
IOB Pull-up Resistors	Enabled	Enabled	Disabled
Device Outputs	Disabled	Disabled	As Configured
Device Inputs and Clocks	Disabled	Disabled	As Configured
Function Block	Disabled	Disabled	As Configured
JTAG Controller	Disabled	Enabled	Enabled

Revision History

Version	Date	Revision
3.0	12/14/98	Revised datasheet to reflect new AC characteristics and Internal Timing Parmeters.
4.0	2/10/99	Corrected Figure 3
5.0	9/15/99	Added -10 speed grade to 95288