SPECIFICATION

Character Type Dot Matrix LCD Module

JM162A

● GENERAL SPECIFICATION

Interface with 4-bit or 8-bit MPU(directly connected M6800 serial MPU)

Display Specification

Display color-Display background color: ①STN: Yellow-Green,Blue-Gray, Black-White

②TN: Position,Negative

Polarizer mode: Positive,Negative;Reflective ,Transflective, Transmissive

Viewing angle: 6:00 OR 12:00

Display duty: 1/16 Driving bias: 1/5

Character Generator ROM (CGROM):10080 bits(208 characterX5X8 dots)&(32 character X5X11 dots)

Character Generator RAM (CGRAM): 64 X 8 bits (8 charactersX5X8 dots)

Display Data RAM (DDRAM): 80X8 bits (80 characters max)

Mechanical characteristics (Unit:mm)

Extenal dimension: 84.0X44.0X10.0 (15.0 for LED Backlight)

View area: 61.0X15.8 Character font: 5X7dots+cursor

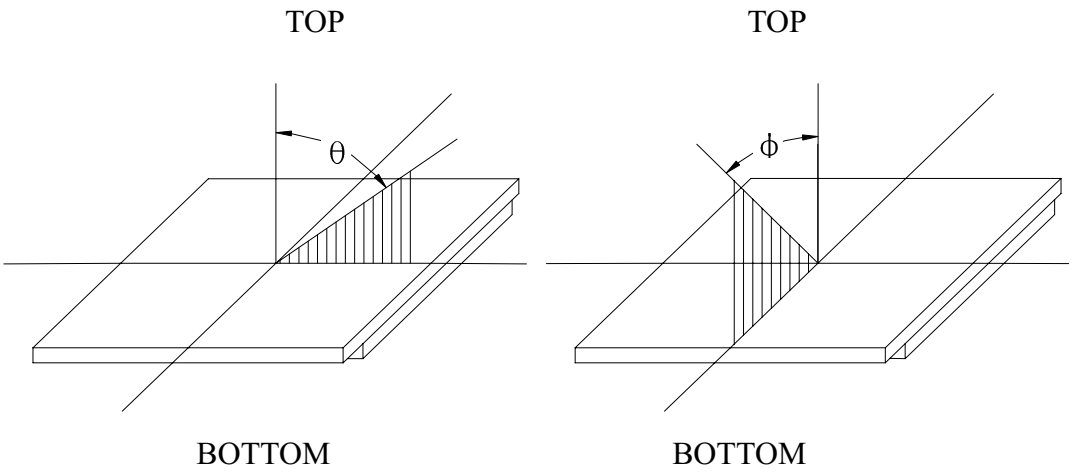
Character size: 2.96X5.56 Dots size: 0.528X0.625

Character pitch: 3.55X6.15

POWER: +5V power

● Optical Characteristics

(1) Definition of viewing Angle



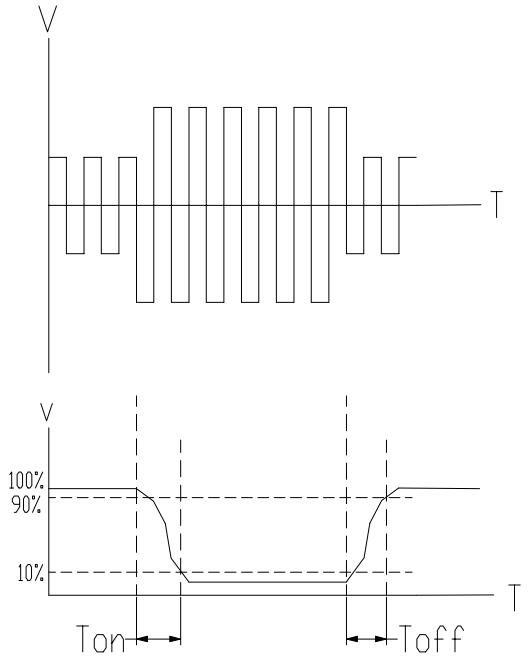
(2) Definition of Contrast Ratio:

$$\text{Contrast Ratio} = \frac{\text{Reflectance value of non-selected state brightness}}{\text{Reflectance value of selected state brightness}}$$

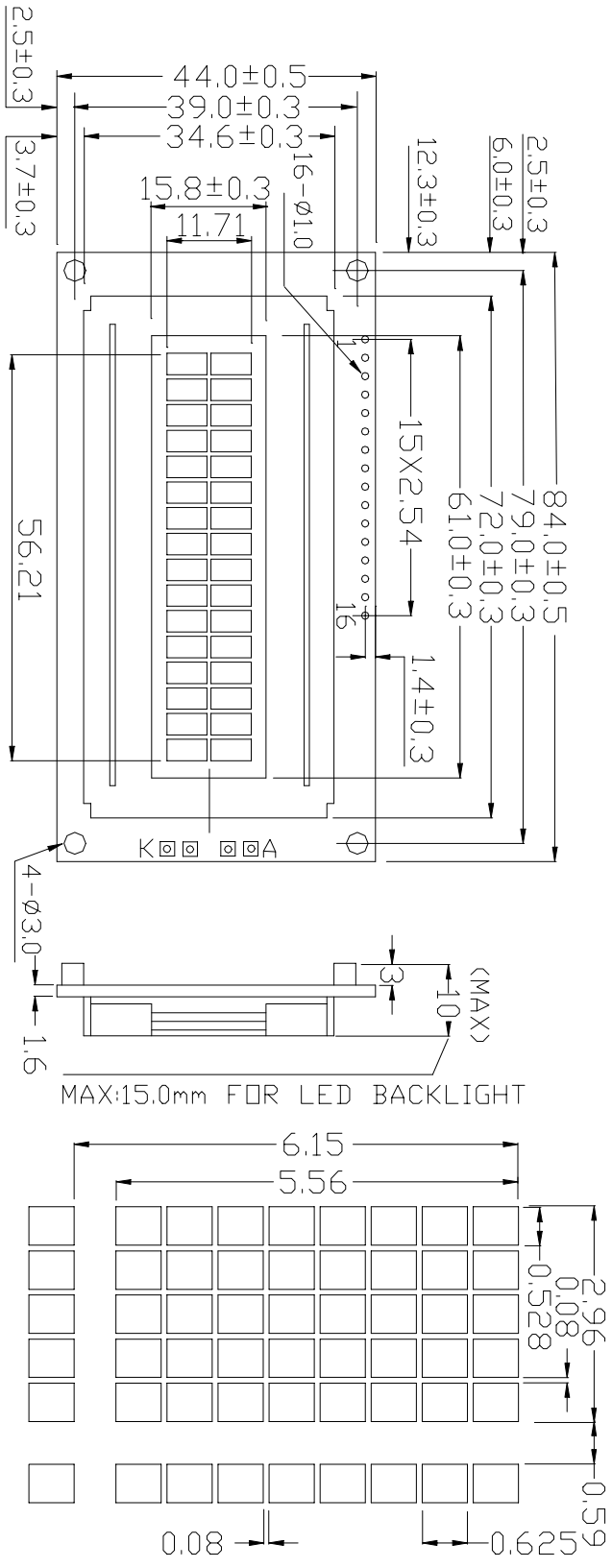
Test condition : standard A light source

(3) Response Time

Response time is measured as the shortest period of time possible between the change in state of an LCD segment as demonstrated below



External Dimension



● Absolute Maximum Ratings

Item	Symbol	Condition	Standard Value		Unit
			Min	Max	
Supply Voltage for logic	Vdd	Ta=25℃	-0.3	7.0	V
Supply Voltage for LCD	V5		Vdd-13.5	0	V
Input Voltage	Vi		-0.3	Vdd+0.3	V
Operating Temperature	Top	-	0	50	℃
Storage Temperature	Tstg	-	-20	70	℃

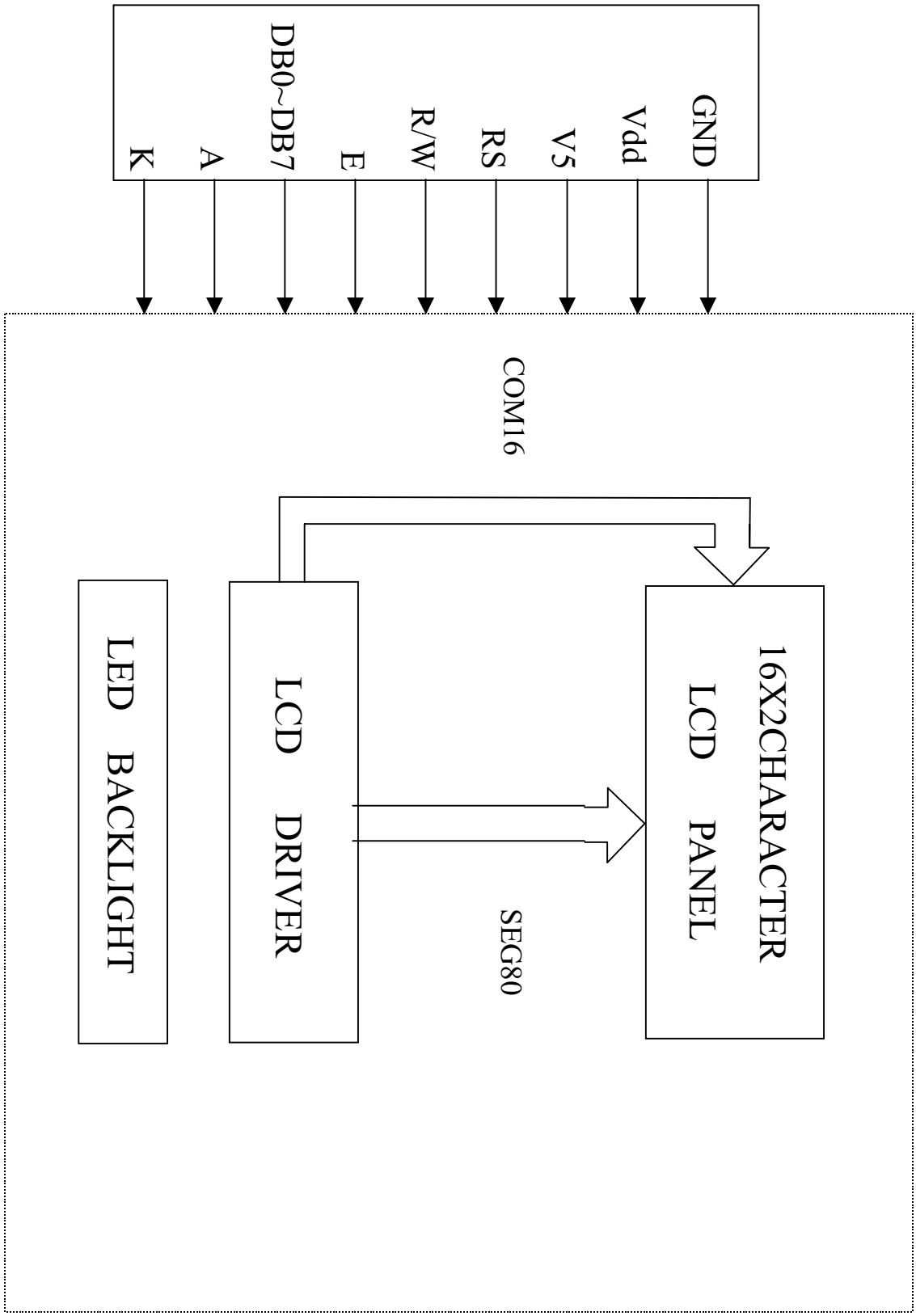
● Electrical Characteristics (Ta=25℃, Vdd= 5.0V)

Item	Symbol	Condition	Standard Value			Unit
			Min	Type	Max	
Supply Voltage for logic	Vdd-GND	-	4.5	5.0	5.5	V
Supply Current for logic	Idd	Vdd=5V	-	1.5	3.0	mA
Driving Current for LCD	Iee		-	0.4	1.0	mA
Driving Voltage for LCD	Vdd-V5		3.8	4.5	4.9	V
Input Voltage H level	Vih		2.2	-	Vdd	V
Input Voltage L level	Vil		-0.3	-	0.6	V
Output Voltage “H”	Voh	Ioh=-0.205mA	2.4	-	-	V
Output Voltage “L”	Vol	Iol=1.2mA	-	-	0.4	V

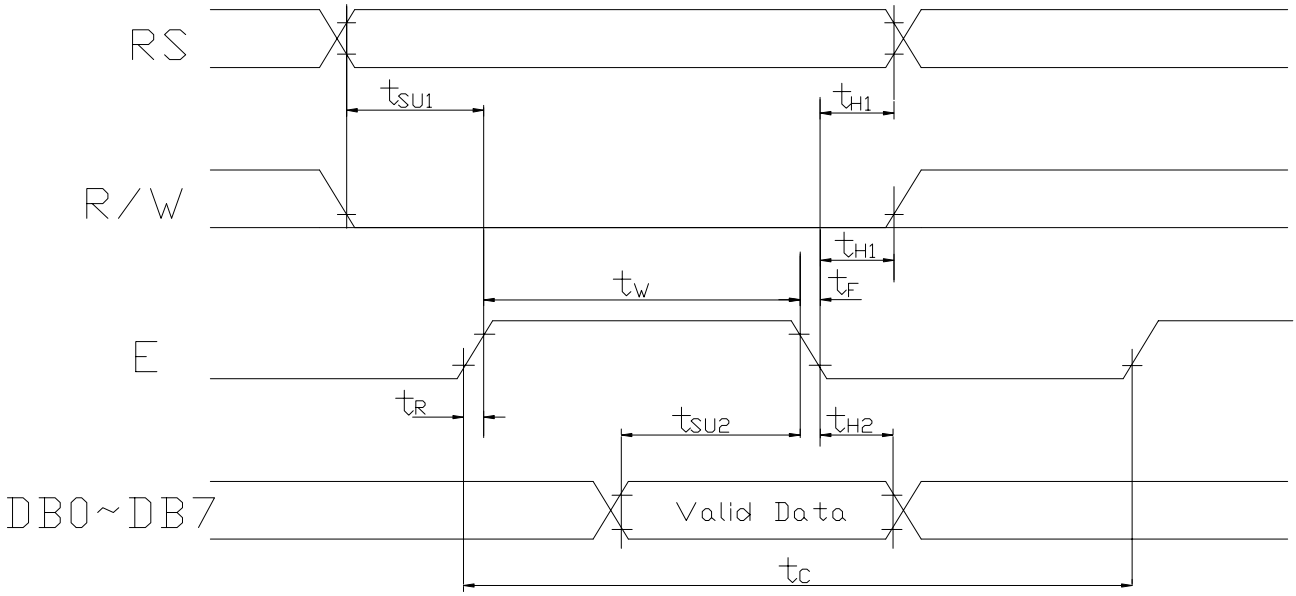
● Absolute Maximum Ratings For LED Backlight

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VLED	If=200mA	-	4.2	-	V
LED Forward Consumption Current	If	Vf=4.2V	-	83	-	mA
LED Allowable Dissipation	Pd	-	-	350	-	mW

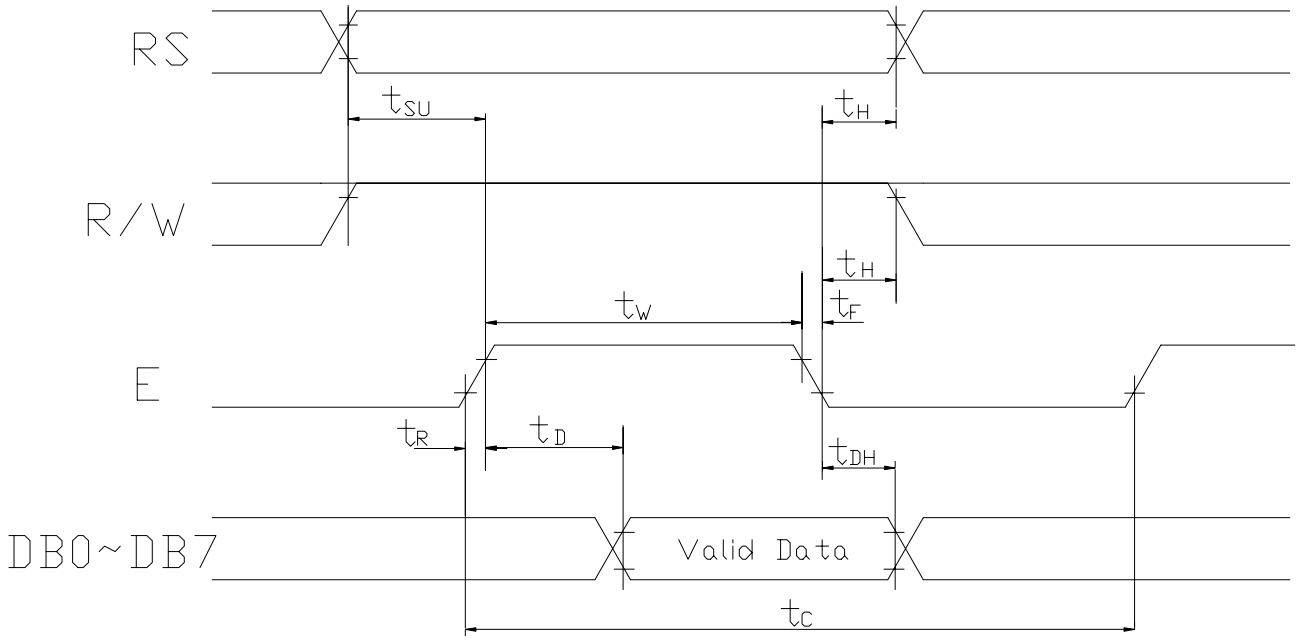
- **Block Diagram**



● Bus Timing



Write Mode Timing Diagram



Read Mode Timing Diagram

● AC Characteristics (Vdd=4.5V~5.5V,Ta=-30~+85℃)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode	E Cycle Time	t_C	500	-	-	ns
	E Rise/Fall Time	$t_{R,}t_F$	-	-	20	
	E Pulse Width (High,Low)	t_W	230	-	-	
	R/W and RS Setup Time	t_{SU1}	40	-	-	
	R/W and RS Hold Time	t_{H1}	10	-	-	
	Data Setup Time	t_{SU2}	80	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode	E Cycle Time	t_C	500	-	-	ns
	E Rise/Fall Time	$t_{R,}t_F$	-	-	20	
	E Pulse Width (High,Low)	t_W	230	-	-	
	R/W and RS Setup Time	t_{SU}	40	-	-	
	R/W and RS Hold Time	t_H	10	-	-	
	Data Output Delay Time	t_D	-	-	120	
	Data Hold Time	t_{DH}	5	-	-	

● IC Specifications

See The Reference of Samsung Data Book-----KS0070B

● Pin assignment

Pin NO.	Symbol	Function		Remark
1	GND	Power supply	0V	
2	Vdd		+5V	
3	V5		For LCD	Variable
4	RS	Register Select(H=Data,L=Instruction)		
5	R/W	Read/Write L=MPU to LCM,H=LCM to MPU		
6	E	Enable		
7	DB0	Data bus bit 0		
8	DB1	Data bus bit 1		
9	DB2	Data bus bit 2		
10	DB3	Data bus bit 3		
11	DB4	Data bus bit 4		
12	DB5	Data bus bit 5		
13	DB6	Data bus bit 6		
14	DB7	Data bus bit 7		
15	A	Anode of LED Unit		
16	K	Cathode of LED Unit		

● Reflector of Screen and DDRAM Address

Display position	1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9	1-10
DDRAM address	00	01	02	03	04	05	06	07	08	09
Display position	1-11	1-12	1-13	1-14	1-15	1-16				
DDRAM address	0A	0B	0C	0D	0E	0F	10	11	12	13
Display position										
DDRAM address	14	15	16	17	18	19	1A	1B	1C	1D
Display position										
DDRAM address	1E	1F	20	21	22	23	24	25	26	27
Display position	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10
DDRAM address	40	41	42	43	44	45	46	47	48	49
Display position	2-11	2-12	2-13	2-14	2-15	2-16				
DDRAM address	4A	4B	4C	4D	4E	4F	50	51	52	53
Display position										
DDRAM address	54	55	56	57	58	59	5A	5B	5C	5D
Display position										
DDRAM address	5E	5F	60	61	62	63	64	65	66	67

"1-1" means first character of line 1 on screen

● Instruction Table

Instruction	Instruction Code										Description	Execution Time(fosc= 270kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write"20H" to DDRAM set DDRAM address to "00H" from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display	39 μ s
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D) cursor(C) and blinking of cursor(B) on/off	39 μ s
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit,and the direction, without changing DDRAM data	39 μ s
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length(DL:8bit/4bit), number of display line (N:2line/1line) and,display font type F:5X11dots / 5X8dots	39 μ s
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	39 μ s
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	39 μ s
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF The contents of address counter can also be read	0 μ s
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	43 μ s
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	43 μ s

● Instruction Description

A. Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H”(space code) to all DDRAM address,and set DDRAM address to “00H” into AC(address counter).
Return cursor to the original status,namely,bring the cursor to the left edge on the first line of the display.
Make the entry mode increment(I/D=”High”).

B. Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Set DDRAM address to “00H” into the address counter.
Return cursor to its original site and return display to its original status,if shifted.
Contents of DDRAM does not change.

C. Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.
I/D:Increment /decrement of DDRAM address(cursor or blink)
I/D=High,cursor/blink moves to right and DDRAM address is increased by 1.
I/D=low,cursor/blink moves to left and DDRAM address is decreased by 1.
*CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.
SH:Shift of entire display
When DDRAM read (CGRAM read/write) operation or SH=Low,shifting of entire display is not performed.if SH=High, and DDRAM write operation,shift of entire display is performed according to I/D value(I/D=High,shift left,I/D=Low, shift right).

D. Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

D:Display ON/OFF control bit
When D=High, entire display is turned on.
When D=Low, display is turned off,but display data remains in DDRAM.
C:Cursor ON/OFF control bit
When C=High, cursor is turned on.
When C=Low, cursor is disappeared in current display ,but I/D register preserves its data.
B:Cursor Blink ON/OFF control bit
When B=High, cursor blink is on, which performs alternately between all the “High” data and display characters at the cursor position.
When B=Low ,blink is off.

E. Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data.
This instruction is used to correct or search display data.
During 2-line mode display,cursor moves to the 2^{nd} line after the 40^{th} digit of the 1^{st} line.
Note that display shift is performed simultaneously in all the lines.
When displayed data is shifted repeatedly,each line is shifted individually.
When display shift is performed,the contents of the address counter are not changed.

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left,cursor moves according to the display
1	1	Shift all the display to the right,cursor moves according to the display

F. Function set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL:Interface data length control bit
When DL=High, it means 8-bit bus mode with MPU.
When DL=Low, it means 4-bit bus mode with MPU.
When 4-bit bus mode, it needs to transfer 4-bit data twice.
N:Display line number control bit
When N=Low, 1-line display mode is set.
When N=High, 2-line display mode is set.
F:Display font type control bit
When F=Low, 5x8 dots format display mode is set.
When F=High, 5x11 dots format display mode.

G. Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

H. Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode(N=Low),DDRAM address is from “00H” to “4FH”.
In 2-line display mode(N=High),DDRAM address in the 1st line is from “00H” to “27H”,and DDRAM address in the 2nd line is from “40H” to “67H”.

I. Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether IC is in internal operation or not .
If BF is “High”,internal operation is in progress and should wait until BF is to be Low,which by then the next instruction can be performed. In this instruction you can also read the value of the address counter.

J. Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM,and CGRAM,is set by the previous address set instruction(DDRAM address set,CGRAM address set).
RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is automatically increased /decreased by 1,according the entry mode.

K. Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction.If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before read operation,the correct RAM data can be obtained from the second. But the first data would be incorrect,as there is no time margin to transfer RAM data.

In case of DDRAM read operation,cursor shift instruction plays the same role as DDRAM address set instruction,it also transfers RAM data to output data register.

After read operation,address counter is automatically increased/decreased by 1 according to the entry mode.

After CGRAM read operation,display shift may not be executed correctly.

Note:In case of RAM write operation,AC is increased/decreased by 1 as in read operation. At this time,AC indicates the next address position, but only the previous data can be read by the read instruction.

● Relationship between Character Code and CGRAM

Character code	CGRAM Address	CGRAM Data	Pattern number
D7 D6 D5 D4 D3 D2 D1 D0	A5 A4 A3 A2 A1 A0	P7 P6 P5 P4 P3 P2 P1 P0	
0 0 0 0 x 0 0 0	0 0 0 0 0 0	x x x 0 1 1 1 0	pattern 1
	0 0 1	x x x 1 0 0 0 1	
	0 1 0	x x x 1 0 0 0 1	
	0 1 1	x x x 1 1 1 1 1	
	1 0 0	x x x 1 0 0 0 1	
	1 0 1	x x x 1 0 0 0 1	
	1 1 0	x x x 1 0 0 0 1	
	1 1 1	x x x 0 0 0 0 0	
⋮	⋮	⋮	⋮
0 0 0 0 x 1 1 1	0 0 0 0 0 0	x x x 1 0 0 0 1	pattern8
	0 0 1	x x x 1 0 0 0 1	
	0 1 0	x x x 1 0 0 0 1	
	0 1 1	x x x 1 1 1 1 1	
	1 0 0	x x x 1 0 0 0 1	
	1 0 1	x x x 1 0 0 0 1	
	1 1 0	x x x 1 0 0 0 1	
	1 1 1	x x x 0 0 0 0 0	

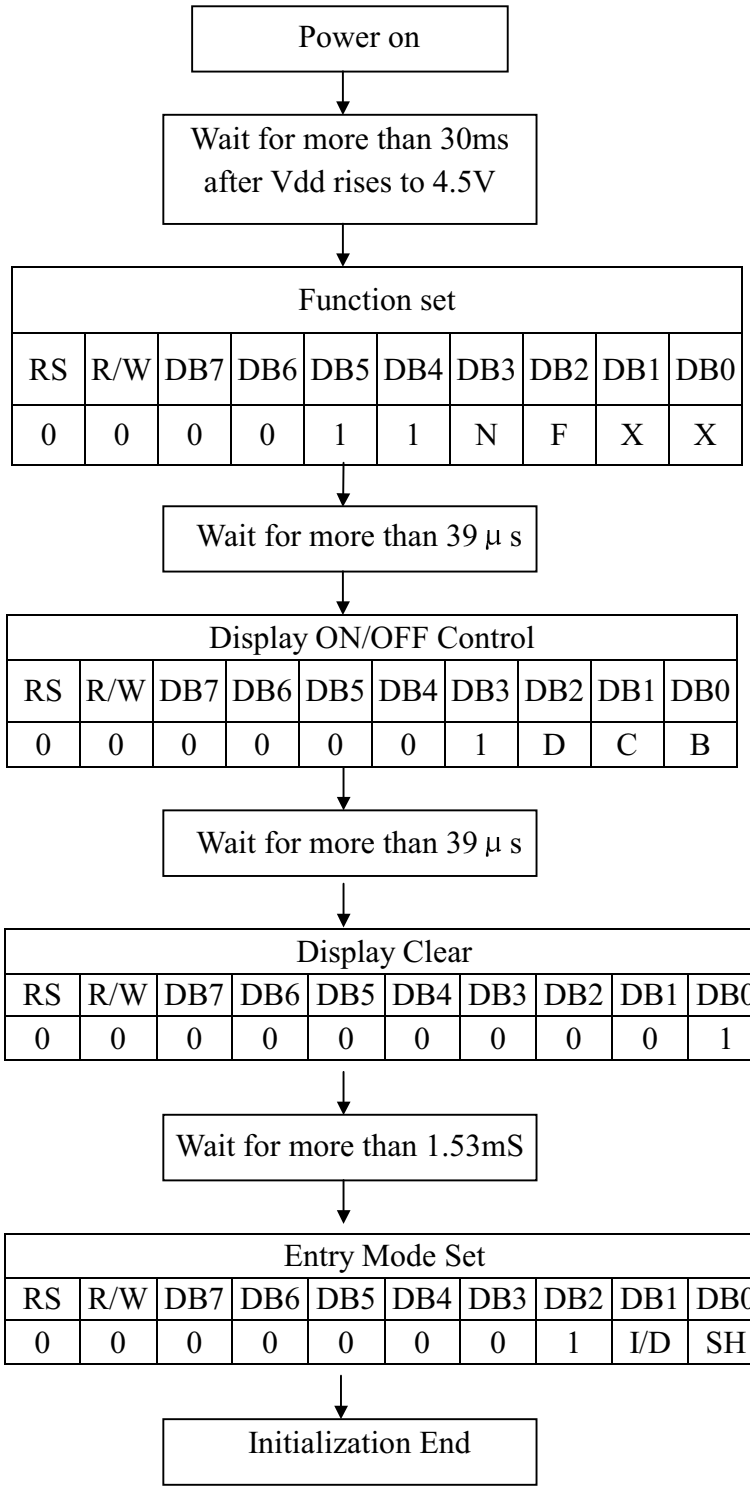
● Display Data RAM(DDRAM)

DDRAM stores display data of maximum 80x8 bits(80 characters).

DDRAM address is set in the address counter(AC) as a hexadecimal number

MSB						LSB
AC6	AC5	AC4	AC3	AC2	AC1	AC0

● Initializing Flowchart(Condition:fosc=270KHZ)



N	0	1-line mode
	1	2-line mode

F	0	5x8 Dots
	1	5x11 Dots

D	0	Display off
	1	Display on

C	0	Cursor off
	1	Cursor on

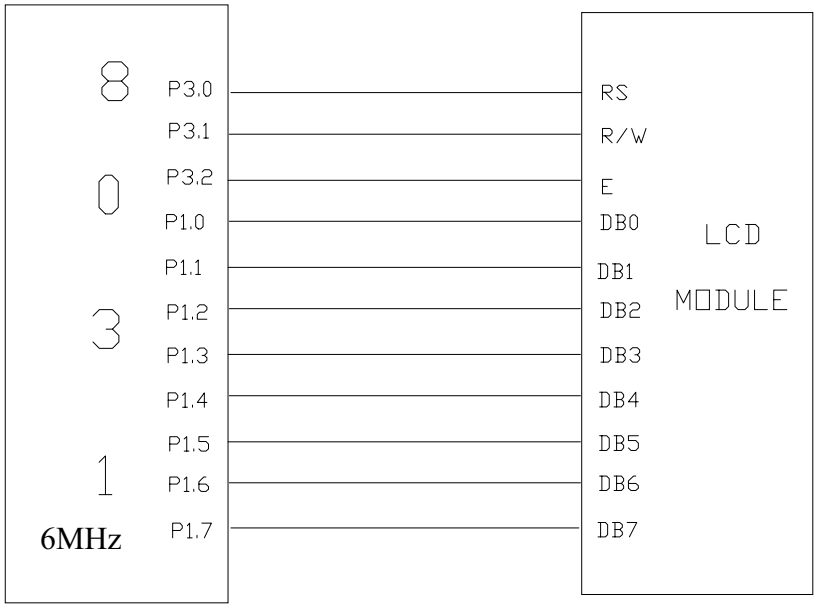
B	0	Blink off
	1	Blink on

I/D	0	Decrement mode
	1	Increment mode

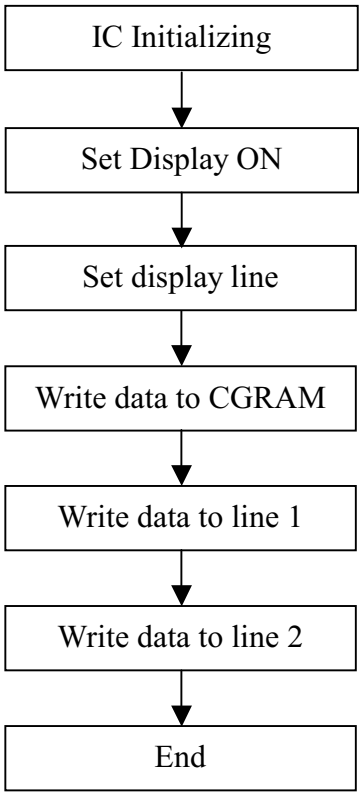
SH	0	Entire shift off
	1	Entire shift on

● Application Example

Application Circuit



Application Flowchart



● Program Example

```
        ORG     0000H
        AJMP MAIN8
MAIN8 : MOV P1,#00H
        CLR P3.0
        CLR P3.1
        CLR P3.2
        LCALL INST0          ;IC Initializing,Set interface data length(8bit),numbers of
                              display line (1line)and ,display font type(5X8dots)
        LCALL OPRN          ;Set display ON
        LCALL INST1          ;Set numbers of display line (2lines)
        LCALL CGROM         ;Write data to CGROM
MAIN :   MOV 30H,#04H
        MOV 31H,#04H
        LCALL MAIN1          ;Call main program
        LJMP MAIN
INST0:  MOV R1,#03H          ; IC Initialed subprogram
ABC:    CLR P3.0
        CLR P3.1
        SETB P3.2
        MOV A,#30H
        MOV P1,A
        CLR P3.2
        LCALL T2
        DJNZ R1,ABC
        RET
OPRN:   CLR P3.0             ; Display ON subprogram
        CLR P3.1
        MOV A,#0CH
        MOV P1,A
        LCALL WRITE
        RET
INST1:  CLR P3.0             ;Set numbers of display line (2lines) subprogram
        CLR P3.1
        MOV A,#38H
        MOV P1,A
        LCALL WRITE
        RET
CGROM:CLR P3.0               ; Write data to CGROM subprogram
        CLR P3.1
```

```
        MOV A,#40H
        MOV P1,A
        LCALL WRITE
        MOV R1,#20H
        SETB P3.0
        CLR P3.1
        MOV DPTR,#TAB2
X1:     CLR A
        MOVC A,@A+DPTR
        MOV P1,A
        LCALL WRITE
        INC DPTR
        DJNZ R1,X1
        RET
MAIN1: MOV DPTR,#TAB1          ;Display TAB1 on screen
        MOV R1,30H
        MOV R2,31H
        LCALL LINE1
        LCALL LINE2
        LCALL T3
        MOV DPTR,#TAB7         ;Display TAB7 on screen
        MOV R1,30H
        MOV R2,31H
        LCALL LINE1
        LCALL LINE2
        LCALL T3
        MOV DPTR,#TAB8         ;Display TAB8 on screen
        MOV R1,30H
        MOV R2,31H
        LCALL LINE1
        LCALL LINE2
        LCALL T3
        MOV DPTR,#TAB9         ;Display TAB9 on screen
        MOV R1,30H
        MOV R2,31H
        LCALL LINE1
        LCALL LINE2
        LCALL T3
        MOV DPTR,#TAB10        ;Display TAB10 on screen
        MOV R1,30H
```

```
        MOV R2,31H
        LCALL LINE1
        LCALL LINE2
        LCALL T3
        MOV DPTR,#TAB11        ;Display TAB11 on screen
        MOV R1,30H
        MOV R2,31H
        LCALL LINE1
        LCALL LINE2
        LCALL T3
        RET
LINE1:  CLR P3.0               ;Write data to line 1
        CLR P3.1
        MOV A,#80H
        MOV P1,A
        LCALL WRITE            ;Set DDRAM address
        SETB P3.0
        CLR P3.1
N1:     MOV R0,#04H
L1:     CLR A
        MOVC A,@A+DPTR
        MOV P1,A
        LCALL WRITE            ;Write data to DDRAM
        INC DPTR
        DJNZ R0,L1
        DJNZ R1,N1
        RET
LINE2:  CLR P3.0               ;Write data on line 2
        CLR P3.1
        MOV A,#0C0H
        MOV P1,A
        LCALL WRITE            ;Set DDRAM address
        CLR P3.1
        SETB P3.0
N2:     MOV R0,#04H
L2:     CLR A
        MOVC A,@A+DPTR
        MOV P1,A
        LCALL WRITE            ;Write data to DDRAM
        INC DPTR
```

```
            DJNZ R0,L2
            DJNZ R2,N2
            RET
WRITE: SETB P3.2                        ;Write subprogram
            MOV R7,#01H
AB:         MOV R6,#0FFH
AC:         DJNZ R6,AC
            DJNZ R7,AB
            CLR P3.2
            RET
T1:         MOV R7,#40H                 ;Delay subprogram 1
AD:         MOV R6,#0FFH
AE:         DJNZ R6,AE
            DJNZ R7,AD
            RET
T2:         MOV R7,#20H                 ;Delay subprogram 2
AF:         MOV R6,#0FFH
AG:         DJNZ R6,AG
            DJNZ R7,AF
            RET
T3:         MOV R7,#03H                 ;Delay subprogram 3
AH:         MOV R6,#8FH
AI:         MOV R5,#0FFH
AJ:         DJNZ R5,AJ
            DJNZ R6,AI
            DJNZ R7,AH
            RET
TAB1:   DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
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            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
TAB2:   DB 1FH,00H,1FH,00H,1FH,00H,1FH,00H
            DB 00H,1FH,00H,1FH,00H,1FH,00H,1FH
            DB 15H,15H,15H,15H,15H,15H,15H,15H
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TAB7:   DB 00H,00H,00H,00H,00H,00H,00H,00H
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        DB 00H,00H,00H,00H,00H,00H,00H,00H
        DB 00H,00H,00H,00H,00H,00H,00H,00H
        DB 00H,00H,00H,00H,00H,00H,00H,00H
        DB 00H,00H,00H,00H,00H,00H,00H,00H
        DB 00H,00H,00H,00H,00H,00H,00H,00H
        DB 00H,00H,00H,00H,00H,00H,00H,00H
        DB 00H,00H,00H,00H,00H,00H,00H,00H
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TAB8:   DB 01H,01H,01H,01H,01H,01H,01H,01H
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        DB 01H,01H,01H,01H,01H,01H,01H,01H
        DB 01H,01H,01H,01H,01H,01H,01H,01H
        DB 01H,01H,01H,01H,01H,01H,01H,01H
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        DB 01H,01H,01H,01H,01H,01H,01H,01H
        DB 01H,01H,01H,01H,01H,01H,01H,01H
        DB 01H,01H,01H,01H,01H,01H,01H,01H
TAB9:   DB 02H,03H,02H,03H,02H,03H,02H,03H
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        DB 02H,03H,02H,03H,02H,03H,02H,03H
        DB 02H,03H,02H,03H,02H,03H,02H,03H
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        DB 02H,03H,02H,03H,02H,03H,02H,03H
TAB10:  DB 03H,02H,03H,02H,03H,02H,03H,02H
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        DB 03H,02H,03H,02H,03H,02H,03H,02H
        DB 03H,02H,03H,02H,03H,02H,03H,02H
        DB 03H,02H,03H,02H,03H,02H,03H,02H
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        DB 03H,02H,03H,02H,03H,02H,03H,02H
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        DB 03H,02H,03H,02H,03H,02H,03H,02H
TAB11:  DB 31H,32H,33H,34H,35H,36H,37H,38H
        DB 39H,41H,42H,43H,44H,45H,46H,47H
        DB 31H,32H,33H,34H,35H,36H,37H,38H
        DB 39H,41H,42H,43H,44H,45H,46H,47H
        DB 31H,32H,33H,34H,35H,36H,37H,38H
        DB 39H,41H,42H,43H,44H,45H,46H,47H
        DB 31H,32H,33H,34H,35H,36H,37H,38H
        DB 39H,41H,42H,43H,44H,45H,46H,47H
        DB 31H,32H,33H,34H,35H,36H,37H,38H
        DB 39H,41H,42H,43H,44H,45H,46H,47H
        END
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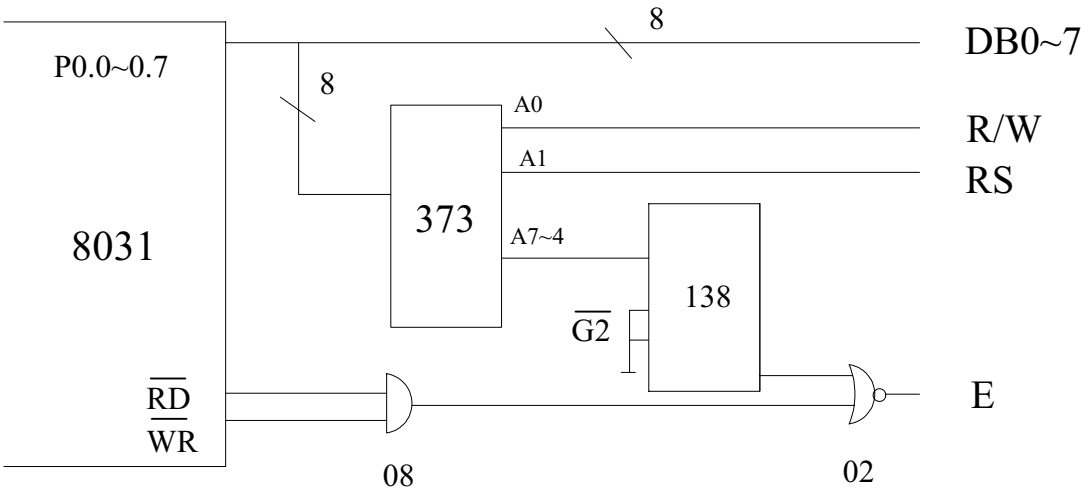
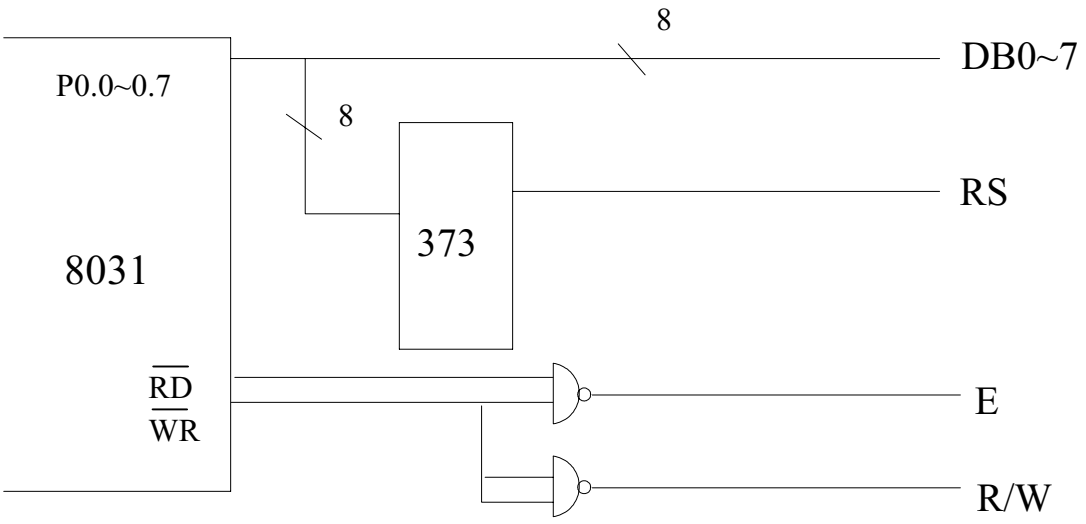
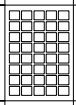
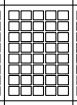
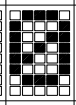
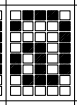
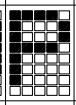
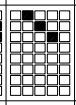
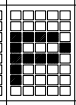
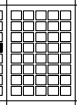
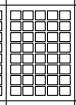
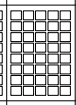
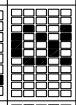
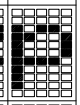
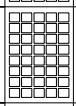
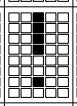
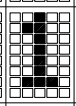
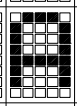
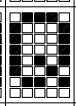
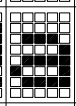
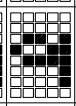
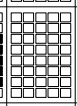
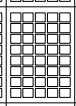
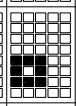
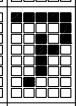
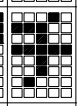
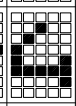
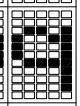
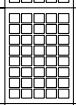
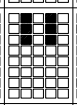
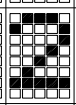
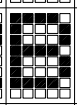
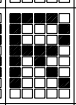
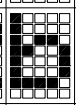
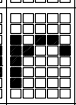
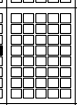
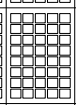
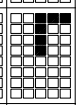
- **Application Circuit 1**



- **Application Circuit 2**



● Character Generator ROM

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
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LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															