SED1330F/1335F/1336F
LCD Controller ICs
Technical Manual

S-MOS Systems, Inc.
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CONTENTS

1.0 Overview 9

1.1 Description 11
1.2 Features 11
1.3 Block Diagram 12
1.4 Pinouts 14
1.4.1 SED1330FBA, 1335FBB and SED1336F0A Pinouts 14
1.4.2 SED1330FBA and SED1335F0A Pinouts 14
1.5 Package Dimensions 15

2.0 Pin Description 17

2.1 SED1330FBA/BB Pin Summary 18
2.2 SED1330F/1335F0A/0B Pin Summary 19
2.3 SED1336F0A Pin Summary 20
2.4 Pin Functions 21
2.4.1 Power Supply 21
2.4.2 Oscillator 21
2.4.3 Microprocessor Interface 21
2.4.4 Display Memory Control 23
2.4.5 LCD Drive Signals 23

3.0 Command Description 25

3.1 The Command Set 27
3.2 System Control Commands 28
3.2.1 SYSTEM SET 28
3.2.1.1 C 29
3.2.1.2 M0 29
3.2.1.3 M1 29
3.2.1.4 M2 29
3.2.1.5 W/S 29
3.2.1.6 IV 32
3.2.1.7 T/L 32
3.2.1.8 DR 32
3.2.1.9 FX 32
3.2.1.10 WF 33
3.2.1.11 FY 33
3.2.1.12 C/R 34
3.2.1.13 TC/R 34
3.2.1.14 L/F 35
3.2.1.15 AP 35
3.2.2 SLEEP IN 36

3.3 Display Control Commands 36
3.3.1 DISP ON/OFF 36
3.3.1.1 D 37
3.3.1.2 FC 37
3.3.1.3 FP 37
3.3.2 SCROLL 37
3.3.2.1 C 37
3.3.2.2 SL1, SL2 38
3.3.3 CSRFORM 42
3.3.3.1 CRX 42
3.3.3.2 CRY 42
3.3.3.3 CM 43
3.3.4 CSRDIR 43
3.3.5 OVLAY 43
3.3.5.1 MX0, MX1 43
3.3.5.2 DM1, DM2 45
3.3.5.3 OV 45
3.3.6 CGRAM ADR 45
3.3.7 HDOT SCR 45
3.3.7.1 D0 to D2 45
3.4 Drawing Control Commands 46
3.4.1 CSRW 46
3.4.2 CSRR 46
3.5 Memory Control Commands 47
3.5.1 MWRITE 47
3.5.2 MREAD 47

4.0 Specifications 49

4.1 Absolute Maximum Ratings 51
4.1.1 SED1330 51
4.1.2 SED1335/SED1336 51
4.2 SED 1330 Electrical Characteristics 52
4.3 SED1335/1336 Electrical Characteristics 53
4.4 SED1330 Timing Diagrams 54
4.4.1 System bus READ/WRITE timing I (8080) 54
4.4.1.1 SED1330F 54
4.4.2 System bus READ/WRITE timing II (6800) 55
4.4.2.1 SED1330F 55
4.4.3 Display memory READ timing 56
4.4.3.1 SED1330F 56
4.4.4 Display memory WRITE timing 57
4.4.4.1 SED1330F 57
4.4.5 LCD control timing 58
4.4.5.1 SED1330F 59

4.4.6 Oscillator timing 60
4.4.6.1 SED1330F 60
4.4.7 Measurement circuit 61
4.5 SED1335/SED1336 AC Timing Diagrams 62
4.5.1 8080 family Interface Timing 62
4.5.1.1 SED1335F 62
4.5.1.2 SED1336F 63
4.5.2 6800 family Interface Timing 64
4.5.2.1 SED1335F 65
4.5.2.2 SED1336F 65
4.5.3 Display Memory Read Timing 66
4.5.3.1 SED1335F 66
4.5.3.2 SED1336F 67
4.5.4 Display Memory Write Timing 68
4.5.4.1 SED1335F 69
4.5.4.2 SED1336F 70
4.5.5 SLEEP IN Command Timing 71
4.5.5.1 SED1335F 71
4.5.5.2 SED1336F 71
4.5.6 External Oscillator Signal Timing 72
4.5.6.1 SED1335F 72
4.5.6.2 SED1336F 72
4.5.7 E-1330 LCD Controller IC 73
4.5.7.1 SED1335F 75
4.5.7.2 SED1336F 75

5.0 Display Control Functions 77

5.1 Character Configuration 79
5.2 Screen Configuration 81
5.2.1 Screen Configuration 81
5.2.2 Display Address Scanning 81
5.2.3 Display Scan Timing 84
5.3 Cursor Control 85
5.3.1 Cursor Register Function 85
5.3.2 Cursor Movement 85
5.3.3 Cursor Display Layers 85
5.4 Memory to Display Relationship 87
5.5 Scrolling 90
5.5.1 On-page Scrolling 90
5.5.2 Inter-page Scrolling 91
5.5.3 Horizontal Scrolling 92
5.5.4 Bidirectional Scrolling 93
5.5.5 Scroll Units 93

6.0 Character Generator 95

6.1 CG Characteristics 97
6.1.1 Internal Character Generator 97
6.1.2 External Character Generator ROM 97
6.1.3 Character Generator RAM 97
6.2 CG Memory Allocation 98
6.3 Setting the Character Generator Address 99
6.3.1 M1 = 1 100
6.3.2 CG RAM Addressing Example 100
6.4 Character Codes 101

7.0 TV Mode (SED1336F only) 103

7.1 Sync Generator Circuit Timing 105

8.0 Description of Circuit Blocks 109

8.1 Microprocessor Interface 111
8.1.1 System Bus Interface 111
8.1.1.1 8080 series 111
8.1.1.2 6800 series 111
8.1.2 Microprocessor Synchronization 111
8.1.2.1 Display Status Indication Output For SED1336F only. 111
8.1.2.2 Internal Register Access 111
8.1.2.3 Display Memory Access 111
8.1.3 Interface Examples 113
8.1.3.1 Z80® to SED1330F/1335F/1336F Interface 113
8.1.3.2 6802 to SED1330F/1335F/1336F Interface 114
8.2 Display Memory Interface 115
8.2.1 Static RAM 115
8.2.2 Supply Current during Display Memory Access 115
8.3 Oscillator Circuit 116
8.4 Status Flag 116
8.5 Reset 117

9.0 Application Notes 119

9.1 Initialization Parameters 121
9.1.1 SYSTEM SET Instruction and Parameters 121
9.1.2 Initialization Example 122
9.1.3 Display Mode Setting Example 1: Combining Text and Graphics 128
9.1.4 Display Mode Setting Example 2: Combining Graphics and Graphics 129
9.1.5 Display Mode Setting Example 3: Combining Three Graphics Layers 130
9.2 System Overview 132

9.3 System Interconnection 133
9.3.1 SED1330F/1335F 133
9.3.2 SED1336F 134
9.4 Smooth Horizontal Scrolling 135
9.5 Layered Display Attributes 137
9.5.1 Inverse Display 137
9.5.2 Half-tone Display 137
9.5.2.1 Menu Pad Display 137
9.5.2.2 Graph Display 138
9.5.3 Flashing Areas 138
9.5.3.1 Small Area 138
9.5.3.2 Large Area 138
9.6 16 × 16-dot Graphic Display 139
9.6.1 Command Usage 139
9.6.2 Kanji Character Display 139

10.0 Internal Character Generator Font 141

11.0 Glossary of Terms 145

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1.0
Overview

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1.0 Overview

1.1 Description

The SED1330/1335F/1336F is a family of versatile LCD controller ICs that can display text and graphics on a medium size LCD panel. The software is compatible among all three chips. S-MOS recommends new designs use the SED1335 since the SED1330 will gradually be replaced by the SED1335.

The SED1336F incorporates a TV sync generator circuit that is compatible with both NTSC and PAL systems. The 256 × 200 pixel TV display comprises three superimposed layers, and is identical to the simultaneous LCD panel display. When driving an LCD only, up to 3 overlapping layers can be displayed on LCD panels up to 640 × 256 pixels in size. The SED1330/1335F does not incorporate a TV controller.

The SED1330/1335F/1336F can display layered text and graphics, scroll the display in any direction and partition the display into multiple screens.

The SED1330/1335F/1336F stores text, character codes and bit-mapped graphics data in external frame buffer memory. Display controller functions include transferring data from the controlling microprocessor to the buffer memory, reading memory data, converting data to display pixels and generating timing signals for the buffer memory, TV monitor and LCD panel.

The SED1330/1335F/1336F has an internal character generator with 160, 5 × 7 pixel characters in internal mask ROM. The character generators support up to 64, 8 × 16 pixel characters in external character generator RAM and up to 256, 8 × 16 pixel characters in external character generator ROM.

1.2 Features

- Text, graphics and combined text/graphics display modes
- Three overlapping screens in graphics mode
- 640 × 256 pixel LCD panel display resolution
- Programmable cursor control
- Smooth horizontal and vertical scrolling of all or part of the display
- 1/2-duty to 1/256-duty LCD drive
- Up to 64 Kbytes of external static RAM frame buffer memory
- Internal character generator
- 160, 5 × 7 pixel characters in internal mask-programmed character generator ROM
- Up to 64, 8 × 16 pixel characters in external character generator RAM
- Up to 256, 8 × 16 pixel characters in external character generator ROM
- 6800 and 8080 family microprocessor interfaces
- NTSC and PAL systems compatible (SED1336F only)
- 256 × 200 pixel TV monitor display resolution (SED1336F only)
- Low power consumption—3.5 mA operating current (V_{DD} = 3.5V), 0.05 µA standby current
- 4.5 to 5.5V (SED1330F)
- 2.7 to 5.5V (SED1330F/1335F)
- 3.0 to 5.5V (SED1336F)
- Available in 60-pin QFPs

1.3 Block Diagram

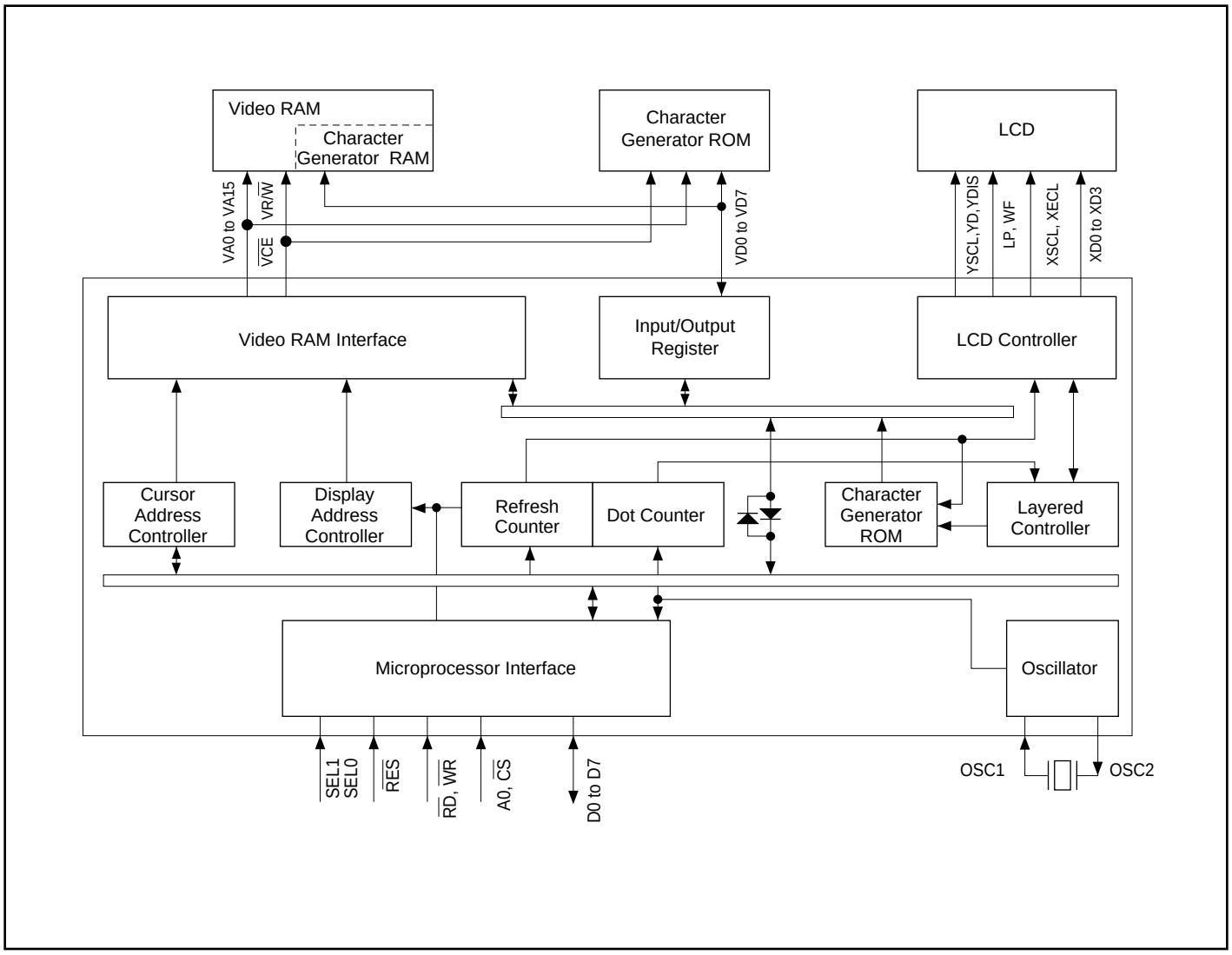

Figure 1. SED1330F block diagram

1.3 Block Diagram

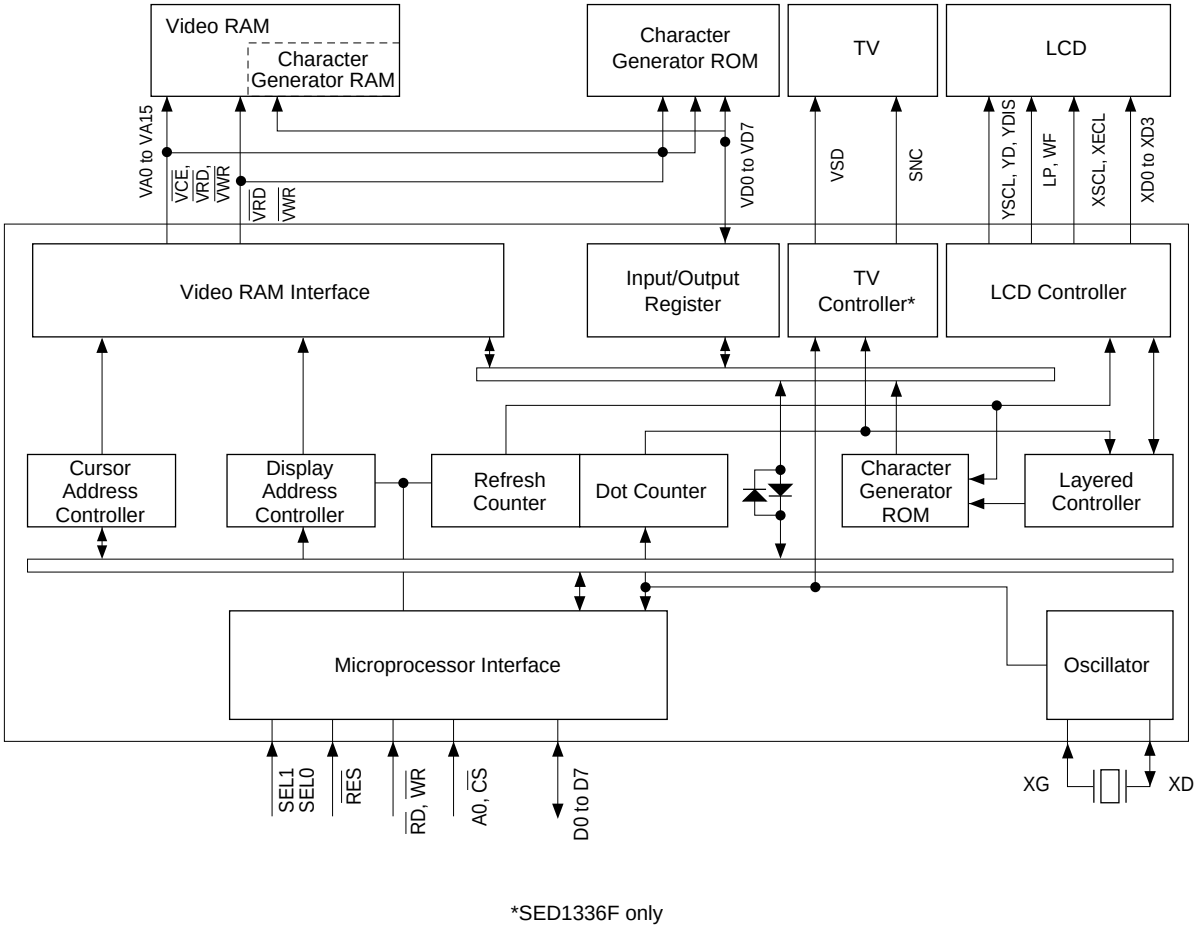

Figure 2. SED1335F/1336F block diagram

1.4 Pinouts

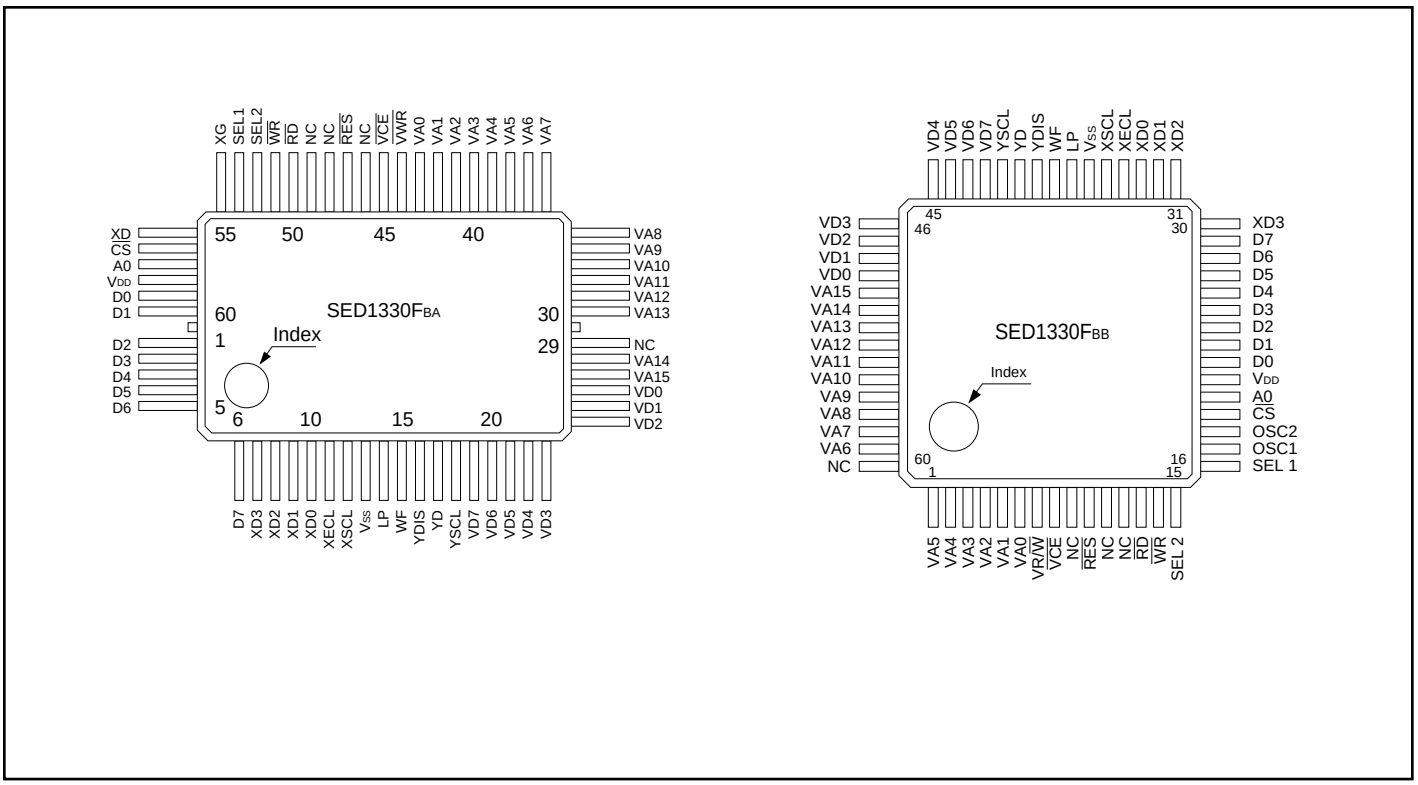

Figure 3. SED1330F and SED1335F pinouts

1.5 Package Dimensions

QFP5

Unit: mm

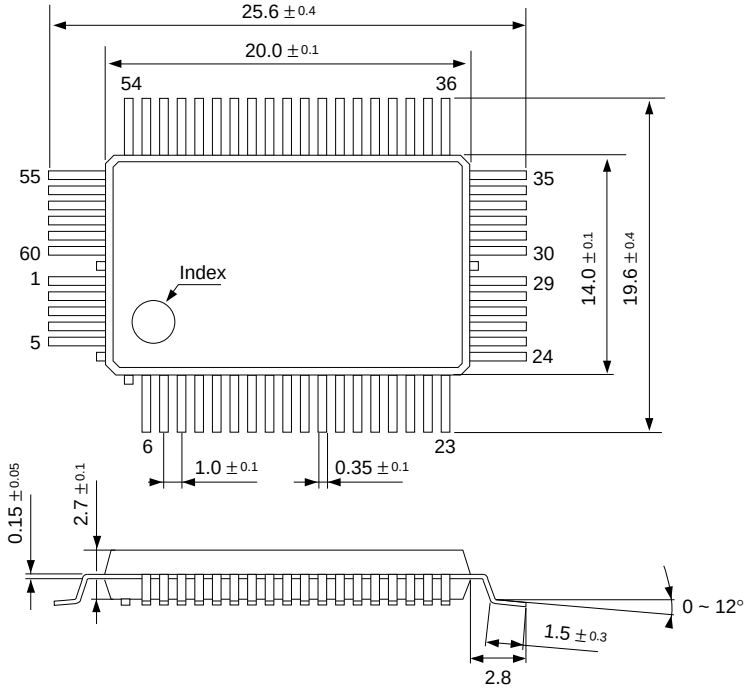

Figure 4. SED1330F_{BA} and 1335F_{0A} package dimensions

QFP6

Unit: mm

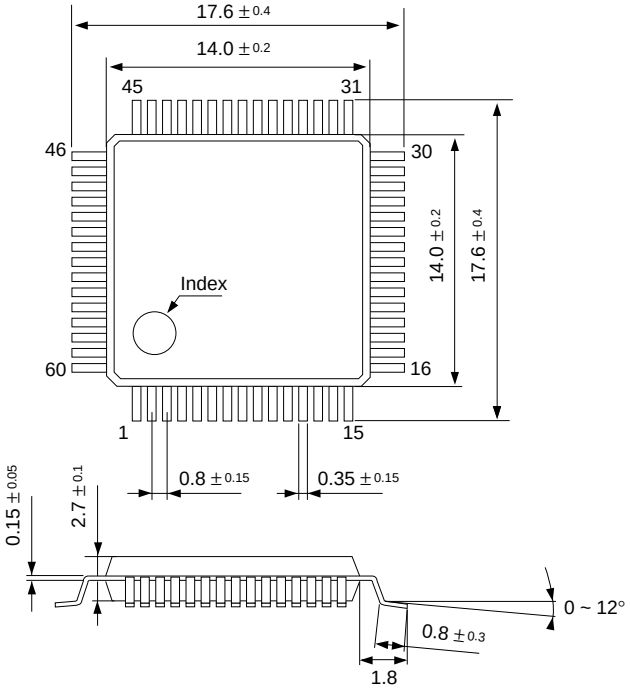

Figure 5. SED1330F_{BB} , 1335F_{0B} and SED1336F_{0A}

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2.0
Pin Description

2.0 Pin Description

2.1 SED1330F$_{BA/BB}$ Pin Summary

Name	Number		Type	Description
	SED1330F$_{0A}$	SED1330F$_{BB}$		
VA0 to VA15	27 to 28 30 to 43	50 to 59 1 to 6	Output	VRAM address bus
VR/$\overline{W}$	44	7	Output	VRAM write signal
$\overline{VCE}$	45	8	Output	Memory control signal
$\overline{RES}$	47	10	Input	Reset
NC	29, 46, 48, 49	9, 11, 12, 60	—	No connection
$\overline{RD}$	50	13	Input	8080 family: Read signal 6800 family: Enable clock (E)
$\overline{WR}$	51	14	Input	8080 family: Write signal 6800 family: R/$\overline{W}$ signal
SEL2	52	15	Input	8080 or 6800 family interface select
SEL1	53	16	Input	8080 or 6800 family interface select
OSC1	54	17	Input	Oscillator connection
OSC2	55	18	Output	Oscillator connection
$\overline{CS}$	56	19	Input	Chip select
A0	57	20	Input	Data type select
V_{DD}	58	21	Supply	4.5 to 5.5V supply
D0 to D7	59 to 60 1 to 6	22 to 29	Input/output	Data bus
XD0 to XD3	10 to 7	33 to 30	Output	X-driver data
XECL	11	34	Output	X-driver enable chain clock
XSCL	12	35	Output	X-driver data shift clock
V_{SS}	13	36	Supply	Ground
LP	14	37	Output	Latch pulse
WF	15	38	Output	Frame signal
YDIS	16	39	Output	Power-down signal when display is blanked
YD	17	40	Output	Scan start pulse
YSCL	18	41	Output	Y-driver shift clock
VD0 to VD7	26 to 19	49 to 42	Input/output	VRAM data bus

2.0 Pin Description

2.2 SED1330F/1335F$_{0A/0B}$ Pin Summary

Name	Number		Type	Description
	SED1335F$_{0A}$	SED1335F$_{0B}$		
VA0 to VA15	27 to 28 30 to 43	50 to 59 1 to 6	Output	VRAM address bus
$\overline{VWR}$	44	7	Output	VRAM write signal
$\overline{VCE}$	45	8	Output	Memory control signal
$\overline{VRD}$	46	9	Output	VRAM read signal
$\overline{RES}$	47	10	Input	Reset
NC	29, 48, 49	11, 12, 60	—	No connection
$\overline{RD}$	50	13	Input	8080 family: Read signal 6800 family: Enable clock (E)
$\overline{WR}$	51	14	Input	8080 family: Write signal 6800 family: R/$\overline{W}$ signal
SEL2	52	15	Input	8080 or 6800 family interface select
SEL1	53	16	Input	8080 or 6800 family interface select
XG	54	17	Input	Oscillator connection
XD	55	18	Output	Oscillator connection
$\overline{CS}$	56	19	Input	Chip select
A0	57	20	Input	Data type select
V_{DD}	58	21	Supply	2.7 to 5.5V supply
D0 to D7	59 to 60 1 to 6	22 to 29	Input/output	Data bus
XD0 to XD3	10 to 7	33 to 30	Output	X-driver data
XECL	11	34	Output	X-driver enable chain clock
XSCL	12	35	Output	X-driver data shift clock
V_{SS}	13	36	Supply	Ground
LP	14	37	Output	Latch pulse
WF	15	38	Output	Frame signal
YDIS	16	39	Output	Power-down signal when display is blanked
YD	17	40	Output	Scan start pulse
YSCL	18	41	Output	Y-driver shift clock
VD0 to VD7	26 to 19	49 to 42	Input/output	VRAM data bus

2.3 SED1336F0A Pin Summary

Name	Number	Type	Description
VA0 to VA15	1 to 6 50 to 59	Output	VRAM address bus
$\overline{VWR}$	7	Output	VRAM write signal
$\overline{VCE}$	8	Output	Memory control signal
$\overline{VRD}$	9	Output	VRAM read signal
$\overline{RES}$	10	Input	Reset
NC	11, 60	—	No connection
CLO	12	Output	Clock output
$\overline{RD}$	13	Input	8080 family: Read signal 6800 family: Enable clock (E)
$\overline{WR}$	14	Input	8080 family: Write signal 6800 family: R/$\overline{W}$ signal
NT/PL	15	Input	NTSC or PAL TV mode select
SEL1	16	Input	8080 or 6800 family interface select
OSC1	17	Input	Oscillator connection
OSC2	18	Output	Oscillator connection
$\overline{CS}$	19	Input	Chip select
A0	20	Input	Data type select
V_{DD}	21	Supply	3.0 to 5.5V supply
D0 to D7	22 to 29	Input/output	Data bus
XD0 to XD3	30 to 33	Output	X-driver data
VSD	34	Output	Video data
XSCL	35	Output	Data shift clock
V_{SS}	36	Supply	Ground
LP	37	Output	Latch pulse
WF	38	Output	Frame signal
YDIS	39	Output	Power-down signal when display is blanked
YD	40	Output	Scan start pulse
SNC	41	Output	TV sync signal
VD0 to VD7	42 to 49	Input/output	VRAM data bus

2.4 Pin Functions

2.4.1 Power Supply

Pin Name	Function
V_{DD}	4.5 to 5.5V (SED1330F), 3.0 to 5.5V (SED1336F) or 2.7 to 5.5V (SED1330F/1335F) supply. This may be the same supply as the controlling microprocessor.
V_{SS}	Ground

Note: The peak supply current drawn by the SED1330F/1335F/1336F may be up to ten times the average supply current. The power supply impedance must be kept as low as possible by ensuring that supply lines are sufficiently wide and by placing 0.47 µF decoupling capacitors that have good high-frequency response near the device's supply pins.

2.4.2 Oscillator

Pin Name	Function
(OSC) XG	Crystal connection for internal oscillator (see Section 8.3). This pin can be driven by an external clock source that satisfies the timing specifications of the EXT ϕ0 signal (see Section 4.3.6).
(OSC2) XD	Crystal connection for internal oscillator. Leave this pin open when using an external clock source.
CLO	Clock output (SED1336F only). Same phase as XG. Clock is output when system command P1 is executed. Output stops during system reset.

2.4.3 Microprocessor Interface

Pin Name	Function
D0 to D7	Tristate input/output pins. Connect these pins to an 8- or 16-bit microprocessor bus.
SEL1, SEL2	Microprocessor interface select pin. The SED1336F supports both 8080 family processors (such as the 8085 and Z80®) and 6800 family processors (such as the 6802 and 6809).

SEL1*	SEL2	Interface	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$
0	0	8080 family	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$
1	0	6800 family	A0	E	R/$\overline{W}$	$\overline{CS}$

* SED1330F and SED1335F only

Note: SEL1 should be tied directly to V_{DD} or V_{SS} to prevent noise. If noise does appear on SEL1, decouple it to ground using a capacitor placed as close to the pin as possible.

<table>
<tr><th>Pin Name</th><th>Function</th></tr>
<tr><td>A0</td><td>A0, in conjunction with the $\overline{RD}$ and $\overline{WR}$ or R/$\overline{W}$ and E signals, controls the type of access to the SED1336F, as shown below.
8080 family interface
<table>
<tr><th>A0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Status flag read</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Display data and cursor address read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Display data and parameter write</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Command write</td></tr>
</table>
6800 family interface
<table>
<tr><th>A0</th><th>R/$\overline{W}$</th><th>E</th><th>Function</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Status flag read</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Display data and cursor address read</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Display data and parameter write</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Command write</td></tr>
</table></td></tr>
<tr><td>$\overline{RD}$ or E</td><td>When the 8080 family interface is selected, this signal acts as the active-LOW read strobe. The SED1330F/1335F/1336F’s output buffers are enabled when this signal is active.
When the 6800 family interface is selected, this signal acts as the active-HIGH enable clock. Data is read from or written to the SED1330F/1335F/1336F when this clock goes HIGH.</td></tr>
<tr><td>$\overline{WR}$ or R/$\overline{W}$</td><td>When the 8080 family interface is selected, this signal acts as the active-LOW write strobe. The bus data is latched on the rising edge of this signal.
When the 6800 family interface is selected, this signal acts as the read/write control signal. Data is read from the SED1330F/1335F/1336F if this signal is HIGH, and written to the SED1330F/1335F/1336F if it is LOW.</td></tr>
<tr><td>$\overline{CS}$</td><td>Chip select. This active-LOW input enables the SED1330F/1335F/1336F. It is usually connected to the output of an address decoder device that maps the SED1330F/1335F/1336F into the memory space of the controlling microprocessor.</td></tr>
<tr><td>$\overline{RES}$</td><td>This active-LOW input performs a hardware reset on the SED1330F/1335F/1336F. It is a Schmitt-trigger input for enhanced noise immunity; however, care should be taken to ensure that it is not triggered if the supply voltage is lowered.</td></tr>
</table>

2.4.4 Display Memory Control

The SED1330F/1335F/1336F can directly access static RAM and PROM. The designer may use a mixture of these two types of memory to achieve an optimum trade-off between low cost and low power consumption.

Pin Name	Function
VA0 to VA15	16-bit display memory address. When accessing character generator RAM or ROM, VA0 to VA3, reflect the lower 4 bits of the row counter.
VD0 to VD7	8-bit tristate display memory data bus. These pins are enabled when VR/$\overline{W}$ is LOW.
VR/$\overline{W}$	Active-LOW display memory write control output (SED1330).
$\overline{VRD}$	Active-LOW display memory read control output (SED1335/6).
$\overline{VCE}$	Active-LOW static memory standby control signal. $\overline{VCE}$ can be used with $\overline{CS}$.
$\overline{VWR}$	Active-LOW display memory write control output (SED1335/6).

2.4.5 LCD Drive Signals

In order to provide effective low-power drive for LCD matrixes, the SED1330F/1335F/1336F can directly control both the X- and Y-drivers using an enable chain.

Pin Name	Function
XD0 to XD3	4-bit X-driver (column drive) data outputs. Connect these outputs to the inputs of the X-driver chips.
XSCL	The falling edge of XSCL latches the data on XD0 to XD3 into the input shift registers of the X-drivers. To conserve power, this clock halts between LP and the start of the following display line (see Section 4.3.7).
XECL	The falling edge of XECL (SED1330F/1335F only) triggers the enable chain cascade for the X-drivers (SED1600/SED1180). Every 16th clock pulse is output to the next X-driver.
LP	LP latches the signal in the X-driver shift registers into the output data latches. LP is a falling-edge triggered signal, and pulses once every display line. Connect LP to the Y-driver shift clock on modules that use the SED1600 and SED1610 drivers.
WF	LCD panel AC drive output. The WF period is selected to be one of two values with SYSTEM SET command.
YSCL	The falling edge of YSCL (SED1330F/1335F only) latches the data on YD into the input shift registers of the Y-drivers. YSCL is not used with the SED1600, SED1610 or other driver ICs which use LP as the Y-driver shift clock.
YD	YD is the data pulse output for the Y drivers. It is active during the last line of each frame, and is shifted through the Y drivers one by one (by YSCL), to scan the display's common connections.
YDIS	Power-down output signal. YDIS is HIGH while the display drive outputs are active. YDIS goes LOW one or two frames after the sleep command is written to the SED1330F/1335F/1336F. All Y-driver outputs are forced to an intermediate level (de-selecting the display segments) to blank the display. In order to implement power-down operation in the LCD unit, the LCD power drive supplies must also be disabled when the display is disabled by YDIS.

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3.0
Command Description

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3.0 Command Description

3.1 The Command Set

Table 1. The Command Set

Class	Command	Code											Hex	Command Description	Command Read Parameters	
		$\overline{RD}$	$\overline{WR}$	A0	D7	D6	D5	D4	D3	D2	D1	D0			No. of Bytes	Section
System control	SYSTEM SET	1	0	1	0	1	0	0	0	0	0	0	40	Initialize device and display	8	3.2.1
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enter standby mode	0	3.2.2
Display control	DISP ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58, 59	Enable and disable display and display flashing	1	3.3.1
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and display regions	10	3.3.2
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor type	2	3.3.3
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start address of character generator RAM	2	3.3.6
	CSRDIR	1	0	1	0	1	0	0	1	1	CD 1	CD 0	4C to 4F	Set direction of cursor movement	0	3.3.4
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position	1	3.3.7
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format	1	3.3.5
Drawing control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address	2	3.4.1
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor address	2	3.4.2
Memory control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory	—	3.5.1
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory	—	3.5.2

Notes:

1. In general, the internal registers of the SED1330F/1335F/1336F are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged.

   2-byte parameters (where two bytes are treated as one data item) are handled as follows:

   a. CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.

   b. SYSTEM SET, SCROLL, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.

2. APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.

3.2 System Control Commands

3.2.1 SYSTEM SET

Initializes the device, sets the window sizes, and selects the LCD interface format. Since the command sets the basic operating parameters of the SED1330F/1335F/1336F, an incorrect SYSTEM SET command may cause other commands to operate incorrectly.

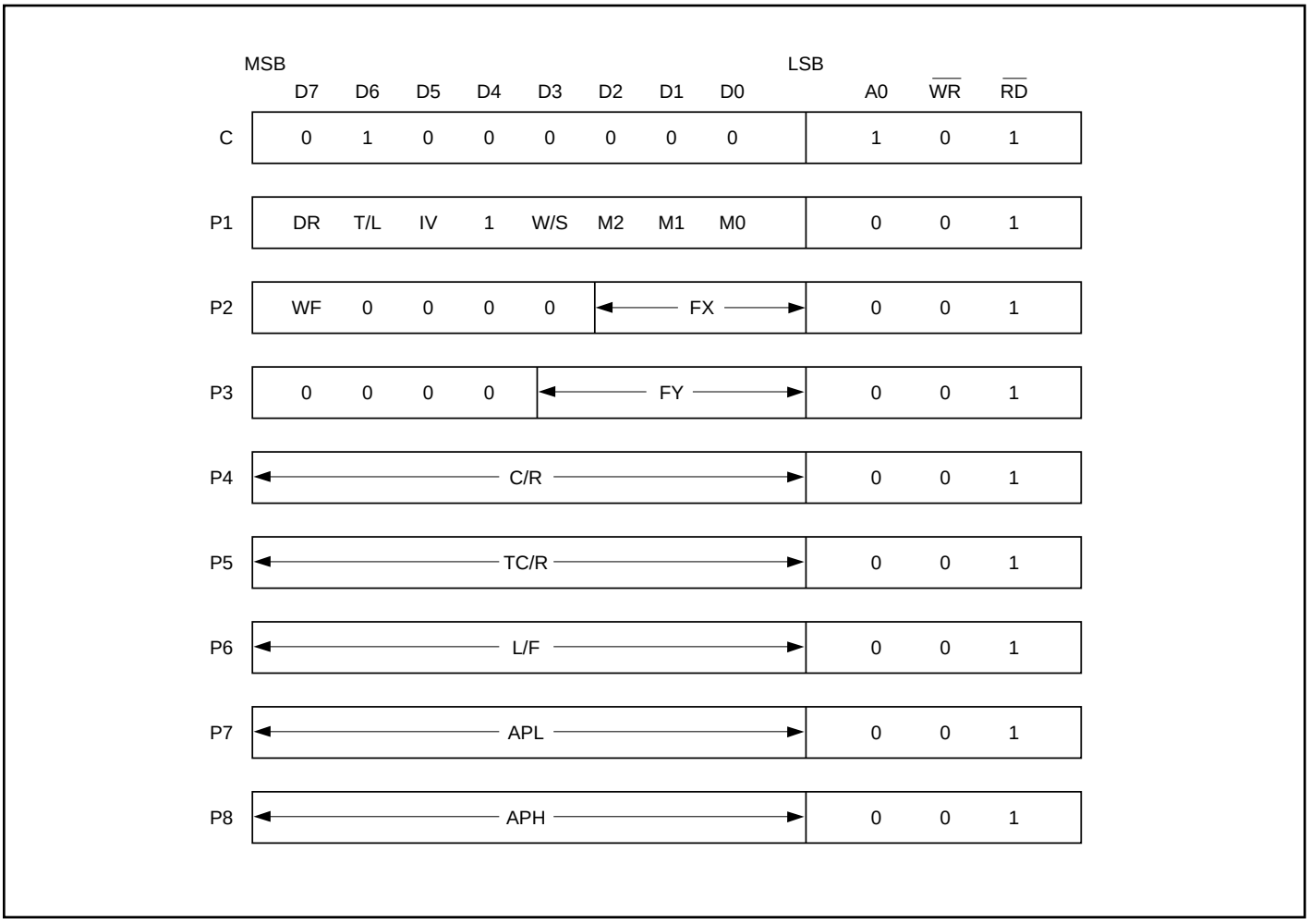


Figure 7. SYSTEM SET instruction

3.2.1.1 C

This control byte performs the following:

1. Resets the internal timing generator
2. Disables the display
3. Cancels sleep mode

Parameters following P1 are not needed if only canceling sleep mode.

3.2.1.2 M0

Selects the internal or external character generator ROM. The internal character generator ROM contains 160, 5×7 pixel characters. These characters are fixed at fabrication by the metalization mask. The external character generator ROM can contain up to 256 user-defined characters.

M0 = 0: Internal CG ROM

M0 = 1: External CG ROM

Note that if the CG ROM address space overlaps the display memory address space, that portion of the display memory cannot be written to.

3.2.1.3 M1

Selects the CG RAM area for user-definable characters. The CG RAM codes are selected from the 64 codes shown in Figure 59.

M1 = 0: CG RAM1; 32 char

The CG RAM1 and CG RAM2 address spaces are not contiguous, the CG RAM1 address space is treated as character generator RAM, and the CG RAM2 address space is treated as character generator ROM.

M1 = 1: 64 char CG RAM + CG RAM2

The CG RAM1 and CG RAM2 address spaces are contiguous and are both treated as character generator RAM.

3.2.1.4 M2

Selects the height of the character defined in external CG ROM and CG RAM. Characters more than 16 pixels high can be displayed by creating a bitmap for each portion of each character and using the SED1330F/1335F/1336F's graphics mode to reposition them.

M2 = 0: 8-pixel character height (2716 or equivalent ROM)

M2 = 1: 16-pixel character height (2732 or equivalent ROM)

3.2.1.5 W/S

Selects the LCD drive method.

W/S = 0: Single-panel drive

W/S = 1: Dual-panel drive

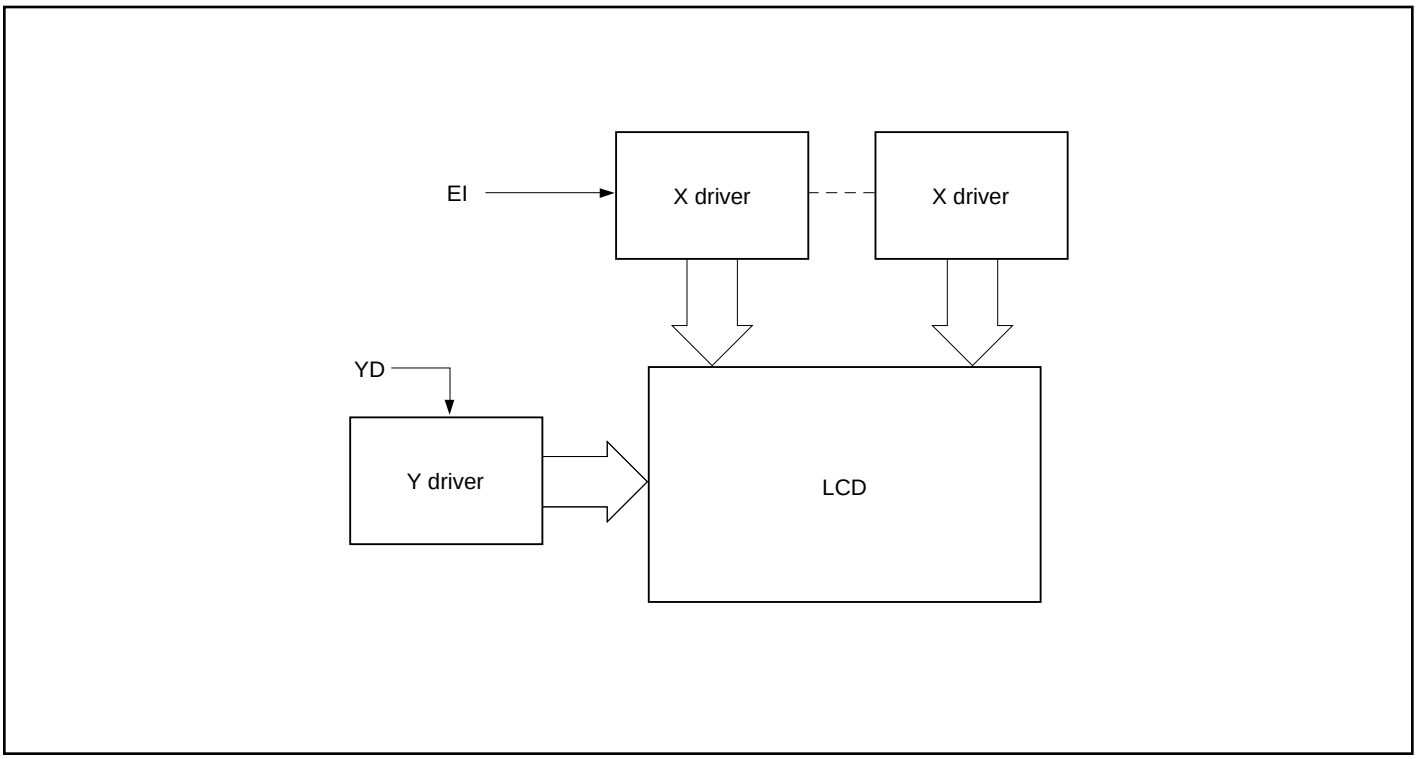


Figure 8. Single-panel display

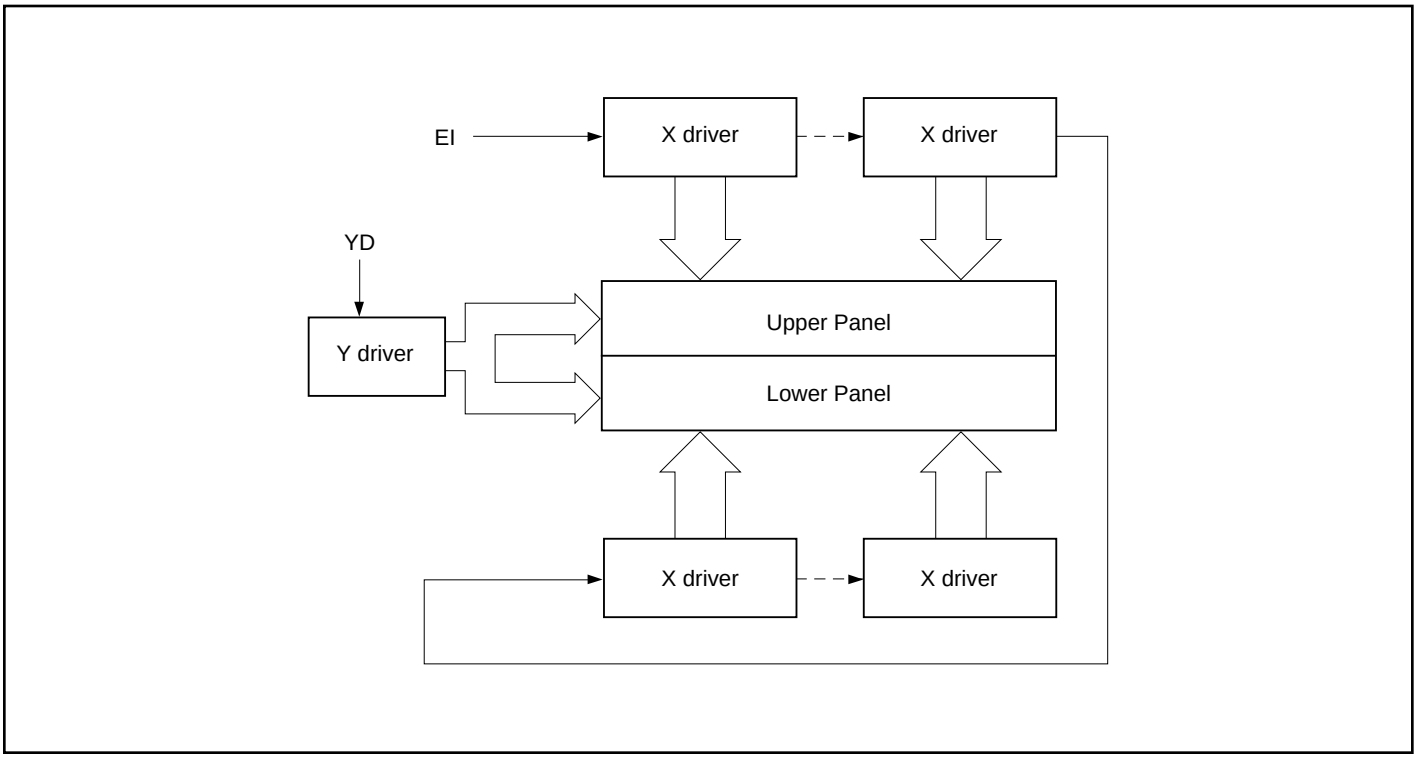
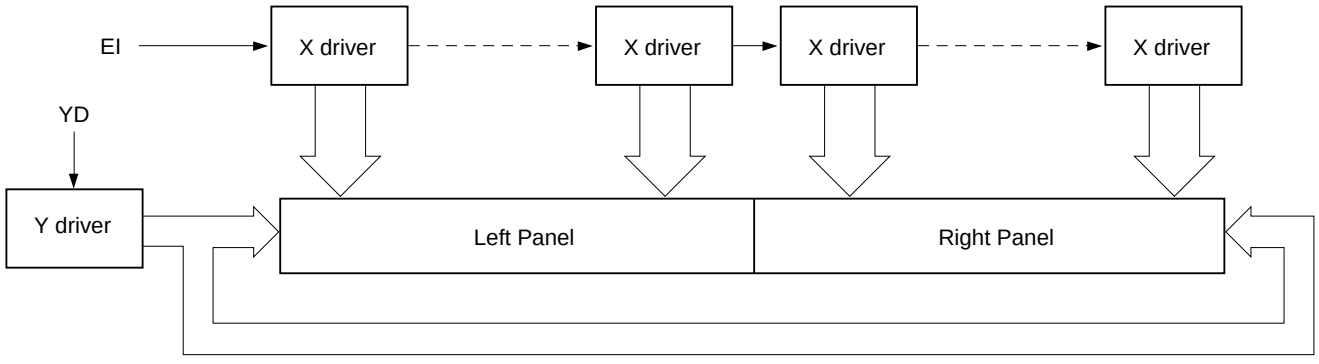


Figure 9. Dual-panel display



Note: There are no Seiko-Epson LCD units in the configuration shown in Figure 10.

Figure 10. Left-and-right two-panel display

Table 3. LCD parameters

Parameter	W/S = 0		W/S = 1	
	IV = 1	IV = 0	IV = 1	IV = 0
C/R	C/R	C/R	C/R	C/R
TC/R	TC/R	TC/R (see note 1)	TC/R	TC/R
L/F	L/F	L/F	L/F	L/F
SL1	00H to L/F	00H to L/F + 1 (see note 2)	(L/F) / 2	(L/F) / 2
SL2	00H to L/F	00H to L/F + 1 (see note 2)	(L/F) / 2	(L/F) / 2
SAD1	First screen block	First screen block	First screen block	First screen block
SAD2	Second screen block	Second screen block	Second screen block	Second screen block
SAD3	Third screen block	Third screen block	Third screen block	Third screen block
SAD4	Invalid	Invalid	Fourth screen block	Fourth screen block
Cursor move-ment range	Continuous movement over whole screen		Above-and-below configuration: continuousmovement over whole screen	

Notes:

1. See table 31 (page 105) for further details on setting the C/R and TC/R parameters when using the HDOT SCR command.
2. The value of SL when IV = 0 is equal to the value of SL when IV = 1, plus one.

3.2.1.6 IV

Screen origin compensation for inverse display. IV is usually set to 1.

The best way of displaying inverted characters is to Exclusive-OR the text layer with the graphics background layer. However, inverted characters at the top or left of the screen are difficult to read as the character origin is at the top-left of its bitmap and there are no background pixels either above or to the left of these characters.

The IV flag causes the SED1330F/1335F/1336F to offset the text screen against the graphics back layer by one vertical pixel. Use the horizontal pixel scroll function (HDOT SCR) to shift the text screen 1 to 7 pixels to the right. All characters will then have the necessary surrounding background pixels that ensure easy reading of the inverted characters.

See Section 5.5 for information on scrolling.

IV = 0: Screen top-line correction

IV = 1: No screen top-line correction (no offset)

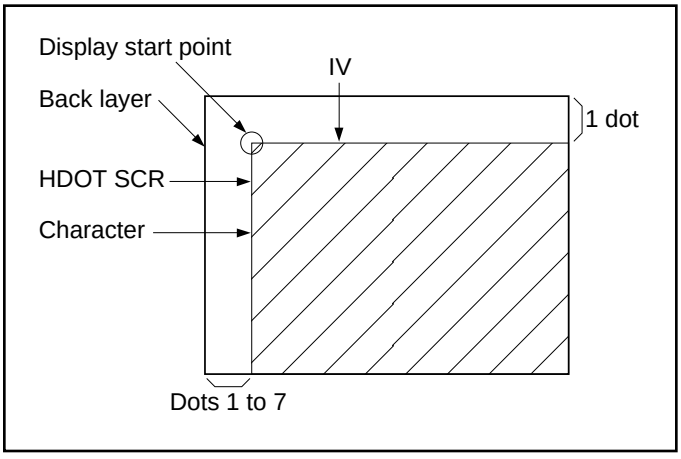


Figure 11. IV and HDOT SCR adjustment

3.2.1.7 T/L

Selects TV or LCD mode. When TV mode is selected, the TV sync generator circuit is ON.

T/L = 0: LCD mode

T/L = 1: TV mode

3.2.1.8 DR

Selects output of an additional shift-clock cycle for every 64 pixels. The extra cycles are required for correct operation of the enable chain when using a two-panel display.

DR = 0: Normal operation

DR = 1: Additional shift-clock cycles

3.2.1.9 FX

Sets the width, in pixels, of the character field. The character width in pixels is equal to FX + 1, where FX can range from 00 to 07H inclusive. If data bit 3 is set (FX is in the range 08 to 0FH) and an 8-pixel font is used, a space is inserted between characters. Note that the maximum character width in TV mode is eight pixels.

Table 4. Horizontal character size selection

FX					[FX] character width (pixels)
HEX	D3	D2	D1	D0	
00	0	0	0	0	1
01	0	0	0	1	2
↓	↓	↓	↓	↓	↓
07	0	1	1	1	8

Since the SED1330F/1335F/1336F handles display data in 8-bit units, characters larger than 8 pixels wide must be formed from 8-pixel segments. As Figure 12 shows, the remainder of the second eight bits are not displayed. This also applies to the second screen layer.

In graphics mode, the normal character field is also eight pixels. If a wider character field is used, any remainder in the second eight bits is not displayed.

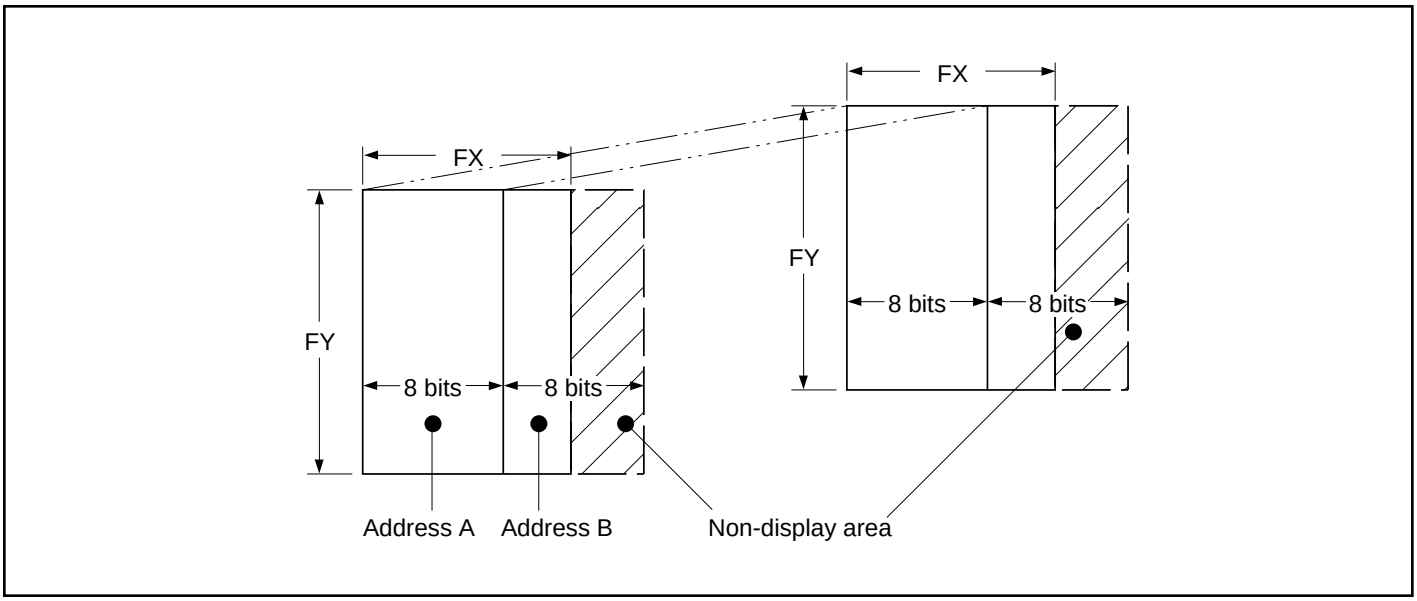


Figure 12. FX and FY display addresses

3.2.1.10 WF

Selects the AC frame drive waveform period. WF is usually set to 1.

WF = 0: 16-line AC drive

WF = 1: two-frame AC drive

In two-frame AC drive, the WF period is twice the frame period.

In 16-line AC drive, WF inverts every 16 lines.

Although 16-line AC drive gives a more readable display, horizontal lines may appear when using high LCD drive voltages or at high viewing angles.

3.2.1.11 FY

Sets the height, in pixels, of the character. The height in pixels is equal to FY + 1.

FY can range from 00 to 0FH inclusive.

Set FY to zero (vertical size equals one) when in graphics mode.

Table 5. Vertical character size selection

FY					[FY] character height (pixels)
HEX	D3	D2	D1	D0	
00	0	0	0	0	1
01	0	0	0	1	2
↓	↓	↓	↓	↓	↓
07	0	1	1	1	8
↓	↓	↓	↓	↓	↓
0E	1	1	1	0	15
0F	1	1	1	1	16

3.2.1.12 C/R

Sets the address range covered by one display line, that is, the number of characters less one, multiplied by the number of horizontal bytes per character.

C/R can range from 0 to 239.

For example, if the character width is 10 pixels, then the address range is equal to twice the number of characters, less 2. See Section 9.1.1 for the calculation of C/R.

[C/R] cannot be set to a value greater than the address range. It can, however, be set smaller than the address range, in which case the excess display area is blank. The number of excess pixels must not exceed 64.

Table 6. Display line address range

C/R									[C/R] bytes per display line
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
4F	0	1	0	0	1	1	1	1	80
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
EE	1	1	1	0	1	1	1	0	239
EF	1	1	1	0	1	1	1	1	240

3.2.1.13 TC/R

Sets the length, including horizontal blanking, of one line. The line length is equal to TC/R + 1, where TC/R can range from 0 to 255.

TC/R must be greater than or equal to C/R + 4. Provided this condition is satisfied, [TC/R] can be set according to the equation given in section 9.1.1 in order to hold the frame period constant and minimize jitter for any given main oscillator frequency, f_{OSC}.

Table 7. Line length selection

TC/R									[TC/R] line length (bytes)
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
52	0	1	0	1	0	0	1	0	83
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

3.2.1.14 L/F

Sets the height, in lines, of a frame. The height in lines is equal to L/F + 1, where L/F can range from 0 to 255.

If W/S is set to 1, selecting two-screen display, the number of lines must be even and L/F must, therefore, be an odd number.

Table 8. Frame height selection

L/F									[L/F] lines per frame
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	0	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

Table 9. Frame heights and compatible LCD units

Number of lines [LF]	Panel Duty Cycle
64	1/64
128	1/64

Table 10. Horizontal address range

Hex code				[AP] addresses per line
APH		APL		
0	0	0	0	0
0	0	0	1	1
↓	↓	↓	↓	↓
0	0	5	0	80
↓	↓	↓	↓	↓
F	F	F	E	$2^{16} – 2$
F	F	F	F	$2^{16} – 1$

3.2.1.15 AP

Defines the horizontal address range of the virtual screen. APL is the least significant byte of the address.

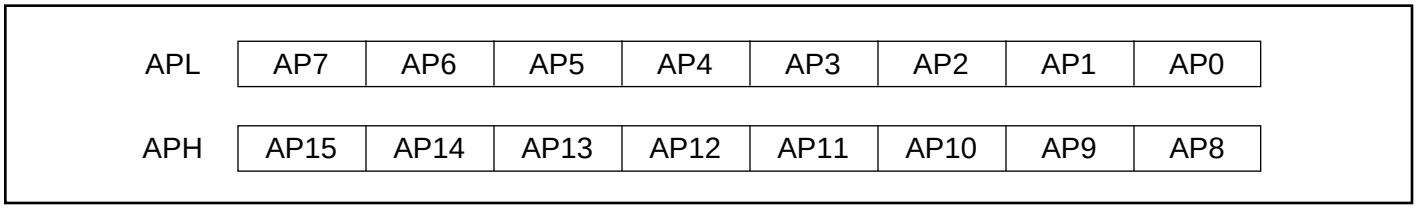


Figure 13. AP parameters

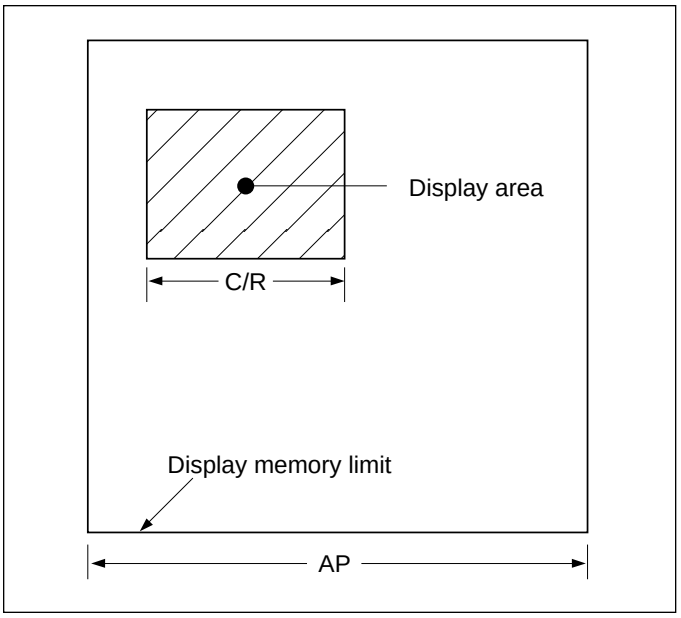


Figure 14. AP and C/R relationship

3.2.2 SLEEP IN

Places the system in standby mode. This command has no parameter bytes. At least one blank frame after receiving this command, the SED1330F/1335F/1336F halts all internal operations, including the oscillator, and enters the sleep mode. Blank data is sent to the X-drivers, and the Y-drivers have their bias supplies turned off by the YDIS signal. Using the YDIS signal to disable the Y-drivers guards against any spurious displays.

The internal registers of the SED1330F/1335/1336F maintain their values during the sleep mode. The display memory control pins maintain their logic levels to ensure that the display memory is not corrupted.

The SED1330F/1335F/1336F can be removed from the sleep state by sending the SYSTEM SET command with only the P1 parameter. The DISP ON command should be sent next to enable the display.

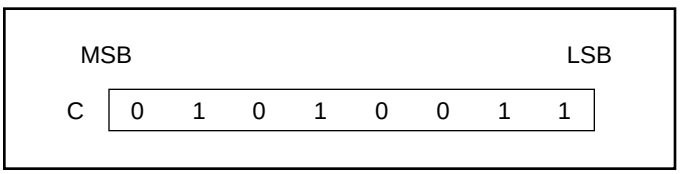


Figure 15. SLEEP IN instruction

1. The YDIS signal goes LOW between one and two frames after the SLEEP IN command is received. Since YDIS forces all display driver outputs to go to the deselected output voltage, YDIS can be used as a power-down signal for the LCD unit. This can be done by having YDIS turn off the relatively high-power LCD drive supplies at the same time as it blanks the display.

2. Since all internal clocks in the SED1330F/1335F/1336F are halted while in the sleep state, a DC voltage will be applied to the LCD panel if the LCD drive supplies remain on.

   If reliability is a prime consideration, turn off the LCD drive supplies before issuing the SLEEP IN command.

3. Note that, although the bus lines become high impedance in the sleep state, pull-up or pull-down resistors on the bus line will force these lines to a known state.

3.3 Display Control Commands

3.3.1 DISP ON/OFF

Turns the whole display on or off. The single-byte parameter enables and disables the cursor and layered screens, and sets the cursor and screen flash rates. The cursor can be set to flash over one character or over a whole line.

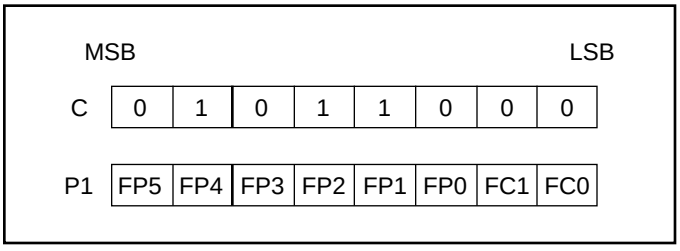


Figure 16. DISP ON/OFF parameters

3.3.1.1 D

Turns the display ON or OFF. The D bit takes precedence over the FP bits in the parameter.

D = 0: Display OFF
D = 1: Display ON

3.3.1.2 FC

Enables/disables the cursor and sets the flash rate. The cursor flashes with a 70% duty cycle (ON/OFF).

Table 11. Cursor flash rate selection

FC1	FC0	Cursor display	
0	0	OFF (blank)	
0	1	ON	No flashing
1	0		Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1		Flash at f_{FR}/64 Hz (approx. 1 Hz)

Note: As the MWRITE command always enables the cursor, the cursor position can be checked even when performing consecutive writes to display memory while the cursor is flashing.

3.3.1.3 FP

Each pair of bits in FP sets the attributes of one screen block, as follows.

Table 12. Screen block attribute selection

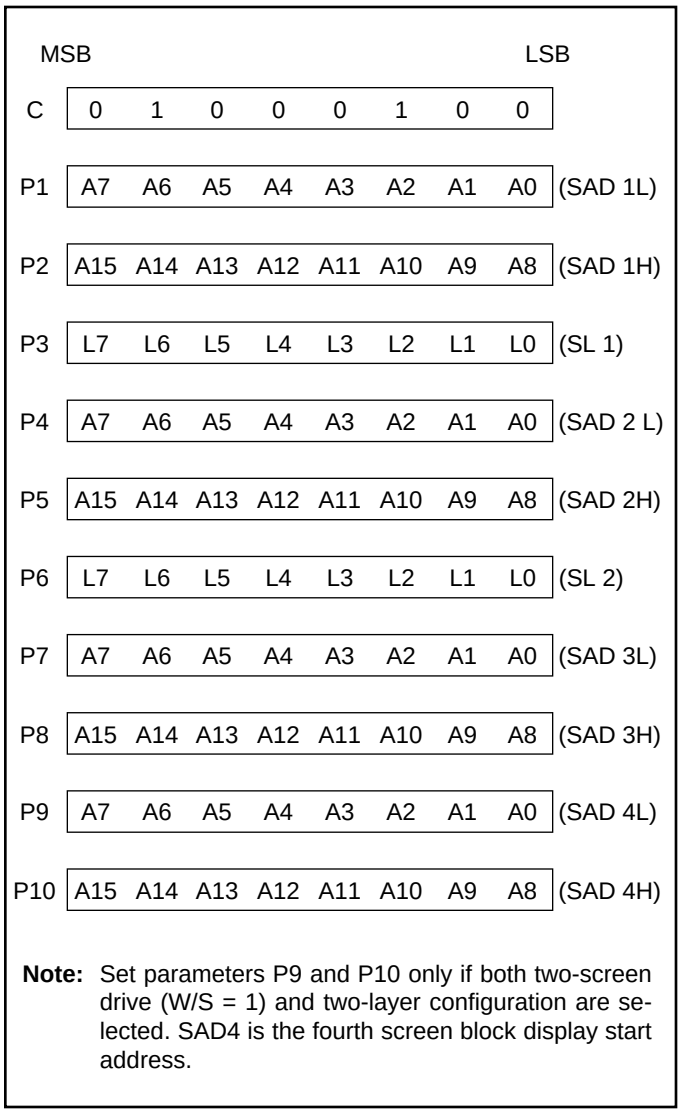
FP1	FP0	First screen block (SAD1)	
FP3	FP2	Second screen block (SAD2, SAD4). See note.	
FP5	FP4	Third screen block (SAD3)	
0	0	OFF (blank)	
0	1	ON	No flashing
1	0		Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1		Flash at f_{FR}/4 Hz (approx. 16 Hz)

Note: If SAD4 is enabled by setting W/S to 1, FP3 and FP2 control both SAD2 and SAD4. The attributes of SAD2 and SAD4 cannot be set independently.

3.3.2 SCROLL

3.3.2.1 C

Sets the scroll start address and the number of lines per scroll block. Parameters P1 to P10 can be omitted if not required. The parameters must be entered sequentially as shown in Figure 17.



Note: Set parameters P9 and P10 only if both two-screen drive (W/S = 1) and two-layer configuration are selected. SAD4 is the fourth screen block display start address.

Figure 17. SCROLL instruction parameters

Table 13. Screen block start address selection

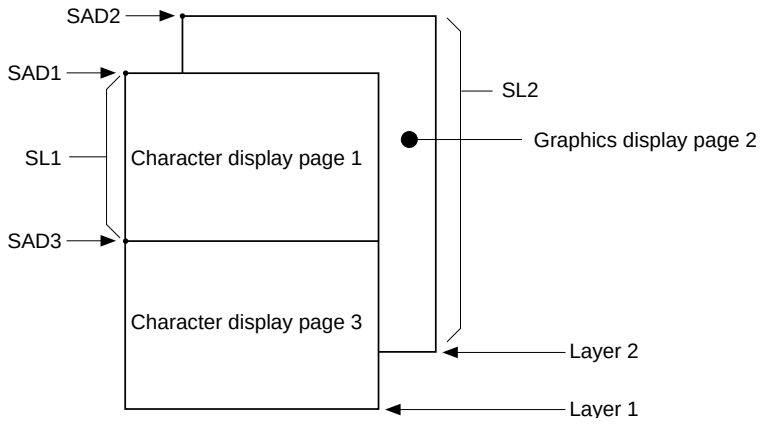
SL1, SL2									[SL] screen lines
HEX	L7	L6	L5	L4	L3	L2	L1	L0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	0	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

3.3.2.2 SL1, SL2

SL1 and SL2 set the number of lines per scrolling screen. The number of lines is SL1 or SL2 plus one.

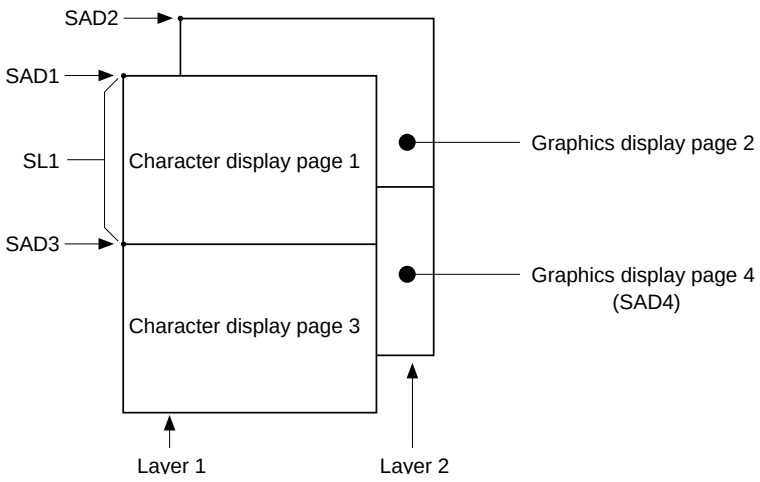
The relationship between SAD, SL and the display mode is described below.

Table 14. Text display mode

W/S	Screen	First Layer	Second Layer
0	First screen block	SAD1	SAD2
	Second screen block	SL1	SL2
	Third screen block (partitioned screen)	SAD3 (see note 1) Set both SL1 and SL2 to L/F + 1 if not using a partitioned screen.	
	Screen configuration example:  		

(continued)

Table 14. Text display mode (continued)

W/S	Screen	First Layer	Second Layer
1	Upper screen	SAD1 SL1	SAD2 SL2
	Lower screen	SAD3 (see note 2)	SAD4 (see note 2)
	Set both SL1 and SL2 to ((L/F) / 2 + 1)		
	Screen configuration example:  		

Notes:

1. SAD3 has the same value as either SAD1 or SAD2, whichever has the least number of lines (set by SL1 and SL2).
2. Since the parameters corresponding to SL3 and SL4 are fixed by L/F, they do not have to be set in this mode.

Table 15. Graphics display mode

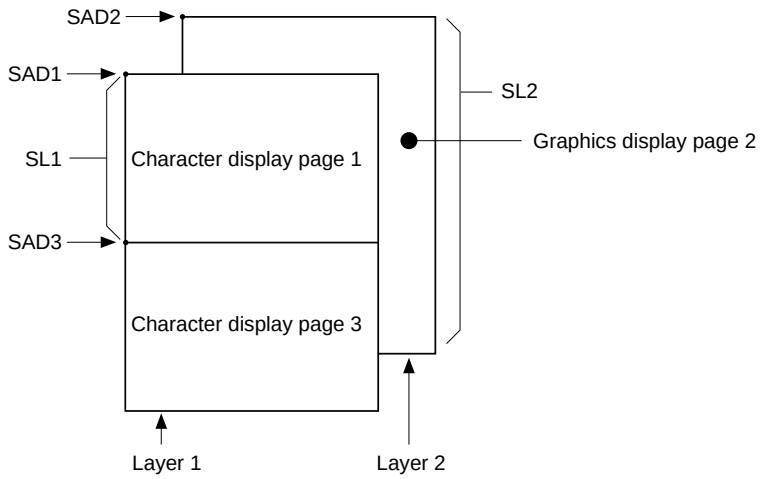
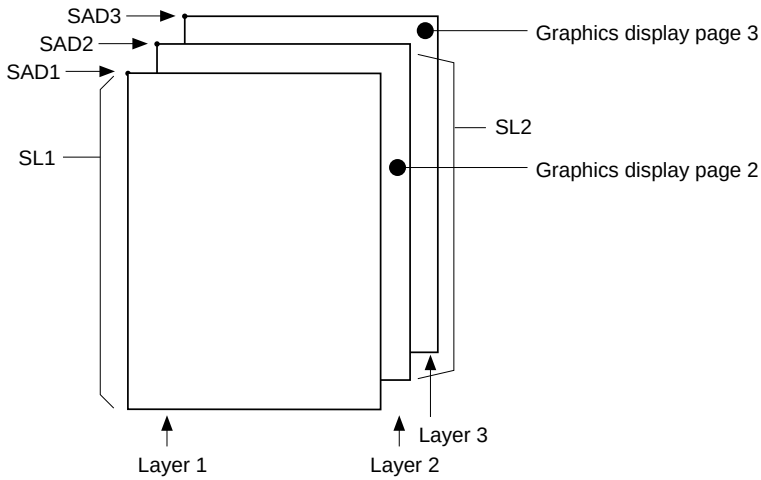
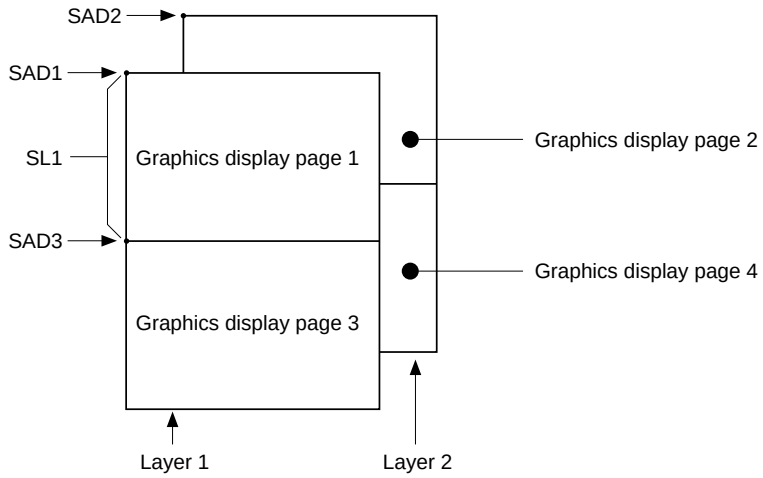
<table>
<tr><th>W/S</th><th>Screen</th><th>First Layer</th><th>Second Layer</th><th>Third Layer</th></tr>
<tr><td rowspan="3">0</td><td>Two-layer composition</td><td>SAD1
SL1</td><td>SAD2
SL2</td><td></td></tr>
<tr><td>Upper screen</td><td colspan="2">SAD3 (see note 3)
Set both SL1 and SL2 to
L/F + 1 if not using a
partitioned screen</td><td></td></tr>
<tr><td colspan="4">Screen configuration example:
 
</td></tr>
<tr><td rowspan="2">0</td><td>Three-layer configuration</td><td>SAD1
SL1 = L/F + 1</td><td>SAD2
SL2 = L/F + 1</td><td>SAD3
—</td></tr>
<tr><td colspan="4">Screen configuration example:
 
</td></tr>
</table>

Table 15. Graphics display mode (continued)

W/S	Screen	First Layer	Second Layer	Third Layer
1	Upper screen	SAD1 SL1	SAD2 SL2	—
	Lower screen	SAD3 (see note 2)	SAD4 (see note 2)	—
	Set both SL1 and SL2 to ((L/F) / 2 + 1)			
	Screen configuration example (see note 3):  			

Notes:

1. SAD3 has the same value as either SAD1 or SAD2, whichever has the least number of lines (set by SL1 and SL2).
2. Since the parameters corresponding to SL3 and SL4 are fixed by L/F, they do not have to be set.
3. If, and only if, W/S = 1, the differences between SL1 and (L/F + 1) / 2, and between SL2 and (L/F + 1) / 2, are blanked.

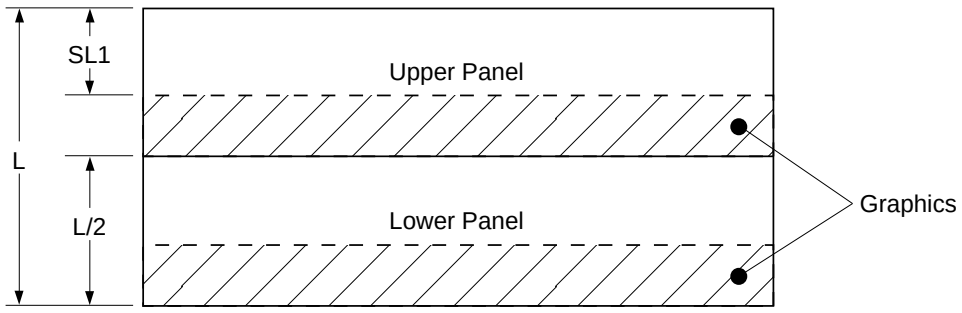


Figure 18. Two-panel display height

3.3.3 CSRFORM

Sets the cursor size and display mode. Although the cursor is normally only used in text displays, it may also be used in graphics displays when displaying special characters.

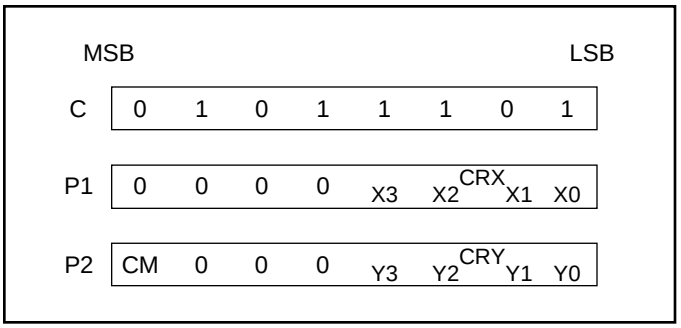


Figure 19. CSRFORM parameter bytes

3.3.3.1 CRX

Sets the horizontal size of the cursor from the character origin. CRX is equal to the cursor size less one. CRX must be less than or equal to FX.

Table 16. Horizontal cursor size selection

CRX					[CRX] cursor width (pixels)
HEX	X3	X2	X1	X0	
0	0	0	0	0	1
1	0	0	0	1	2
↓	↓	↓	↓	↓	↓
8	1	0	0	0	9
↓	↓	↓	↓	↓	↓
E	1	1	1	0	15
F	1	1	1	1	16

3.3.3.2 CRY

Sets the location of an underscored cursor in lines, from the character origin. When using a block cursor, CRY sets the vertical size of the cursor from the character origin. CRY is equal to the number of lines less one.

Table 17. Cursor height selection

CRY					[CRY] cursor height (lines)
HEX	Y3	Y2	Y1	Y0	
0	0	0	0	0	illegal
1	0	0	0	1	2
↓	↓	↓	↓	↓	↓
8	1	0	0	0	9
↓	↓	↓	↓	↓	↓
E	1	1	1	0	15
F	1	1	1	1	16

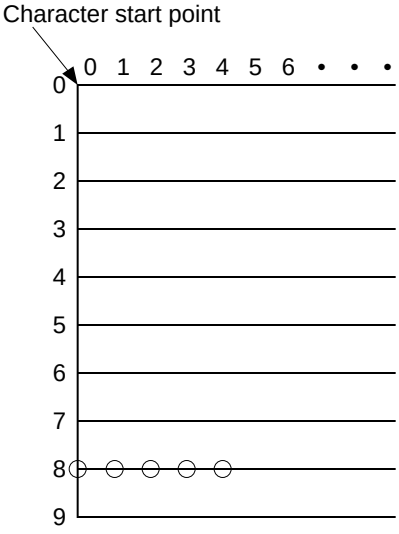


Figure 20. Cursor size and position

3.3.3.3 CM

Sets the cursor display mode. Always set CM to 1 when in graphics mode.

CM = 0: Underline cursor

CM = 1: Block cursor

3.3.4 CSRDIR

Sets the direction of automatic cursor increment. The cursor can move left or right one character, or up or down by the number of bytes specified by the address pitch, AP.

When reading from and writing to display memory, this automatic cursor increment controls the display memory address increment on each read or write.

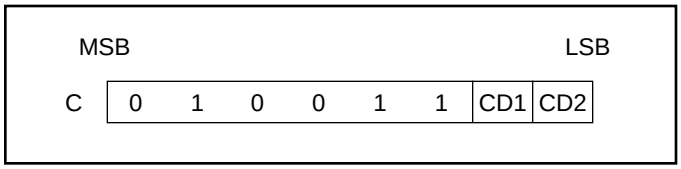


Figure 21. CSRDIR parameters

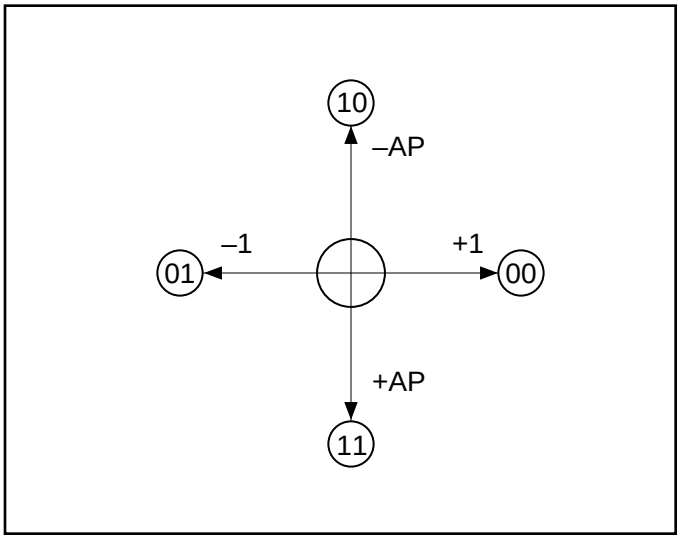


Figure 22. Cursor direction

Table 18. Cursor shift direction

C	CD1	CD0	Shift direction
4CH	0	0	Right
4DH	0	1	Left
4EH	1	0	Up
4FH	1	1	Down

Note: Since the cursor moves in address units even if FX ≥ 9, the cursor address increment must be preset for movement in character units. See Section 5.3.

3.3.5 OVLAY

Selects layered screen composition and screen text/graphics mode.

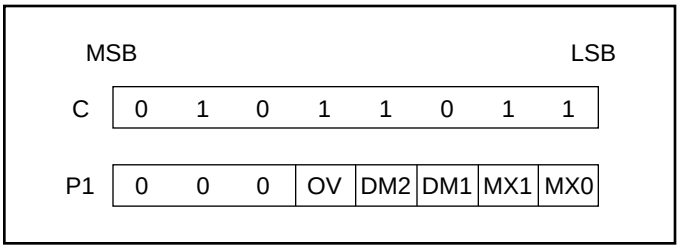


Figure 23. OVLAY parameter

3.3.5.1 MX0, MX1

MX0 and MX1 set the layered screen composition method, which can be either OR, AND, Exclusive-OR or Priority-OR. Since the screen composition is organized in layers and not by screen blocks, when using a layer divided into two screen blocks, different composition methods cannot be specified for the individual screen blocks.

The Priority-OR mode is the same as the OR mode unless flashing of individual screens is used.

Table 19. Composition method selection

MX1	MX0	Function	Composition Method	Applications
0	0	L1 ∪ L2 ∪ L3	OR	Underlining, rules, mixed text and graphics
0	1	(L1 ⊕ L2) ∪ L3	Exclusive-OR	Inverted characters, flashing regions, underlining
1	0	(L1 ∩ L2) ∪ L3	AND	Simple animation, three-dimensional appearance
1	1	L1 > L2 > L3	Priority-OR	

Notes:

L1: First layer (text or graphics). If text is selected, layer L3 cannot be used.

L2: Second layer (graphics only)

L3: Third layer (graphics only)

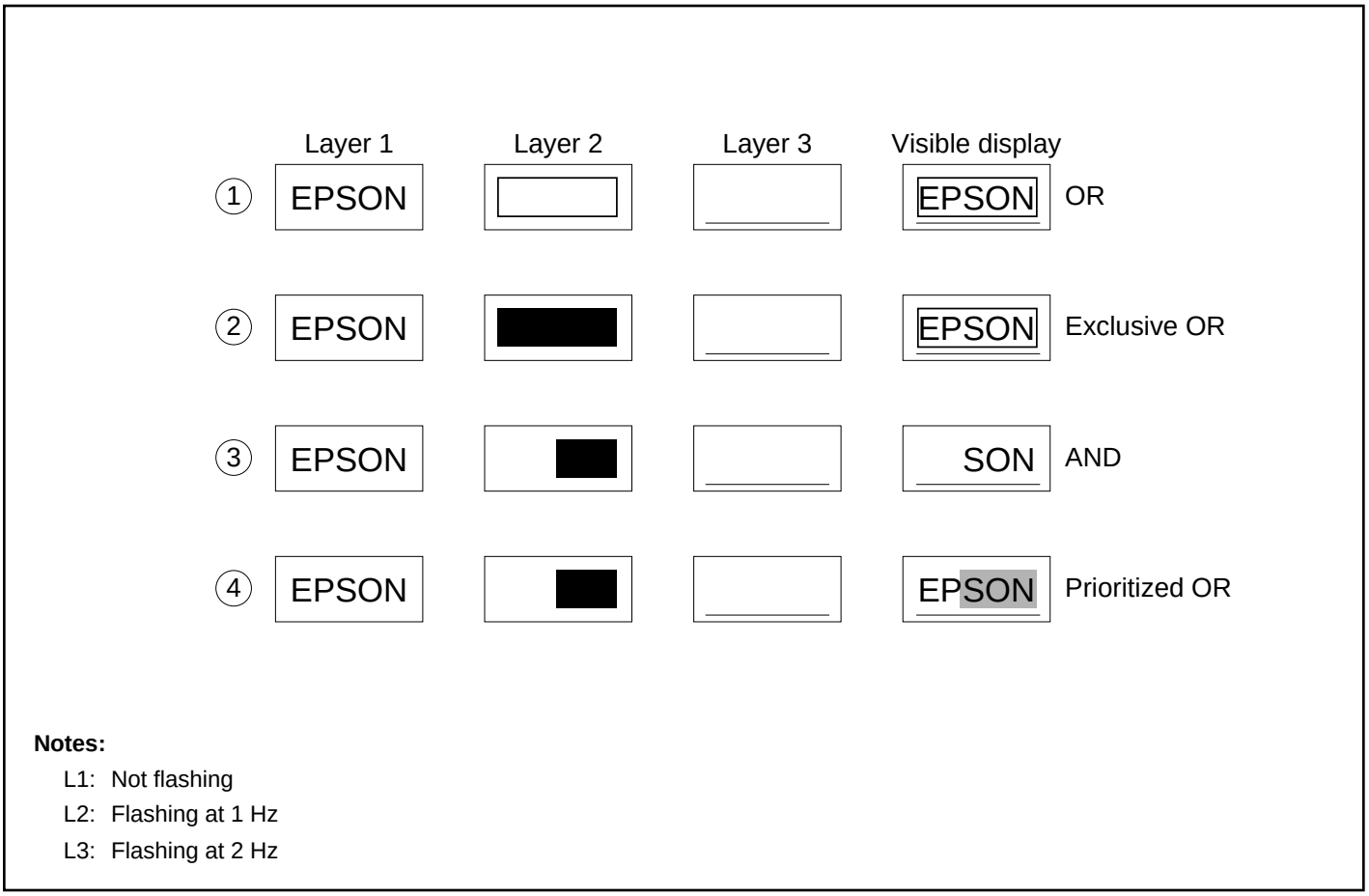


Figure 24. Combined layer display

3.3.5.2 DM1, DM2

DM1 and DM2 specify the display mode of screen blocks 1 and 3, respectively.

DM1/2 = 0: Text mode

DM1/2 = 1: Graphics mode

Note 1: Screen blocks 2 and 4 can only display graphics.

Note 2: DM1 and DM2 must be the same, regardless of the setting of W/S.

3.3.5.3 OV

Specifies two- or three-layer composition in graphics mode.

OV = 0: Two-layer composition

OV = 1: Three-layer composition

Set OV to 0 for mixed text and graphics mode.

3.3.6 CGRAM ADR

Specifies the CG RAM start address.

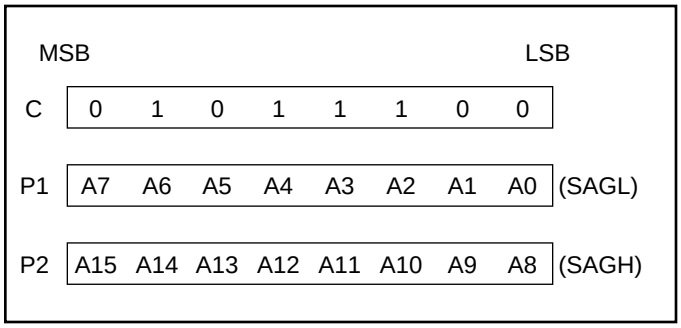


Figure 25. CGRAM ADR parameters

Note: See Section 6 for information on the SAG parameters.

3.3.7 HDOT SCR

While the scroll command only allows scrolling by characters, HDOT SCR allows the screen to be scrolled horizontally by pixels. HDOT SCR cannot be used on individual layers.

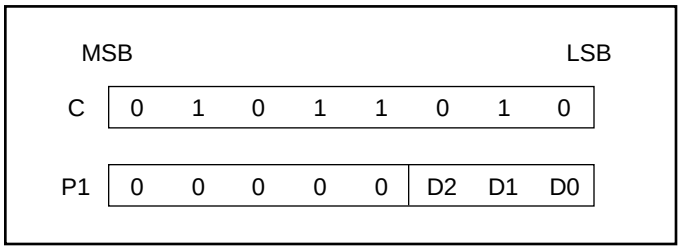


Figure 26. HDOT SCR parameters

3.3.7.1 D0 to D2

Specifies the number of pixels to scroll. The C/R parameter has to be set to one more than the number of horizontal characters before using HDOT SCR. Smooth scrolling can be simulated if the controlling microprocessor repeatedly issues the HDOT SCR command to the SED1330F/1335F/1336F. See Section 5.5 for more information on scrolling the display.

Table 20. Scroll step selection

P1				Number of pixels to scroll
HEX	D2	D1	D0	
00	0	0	0	0
01	0	0	1	1
02	0	1	0	2
↓	↓	↓	↓	↓
06	1	1	0	6
07	1	1	1	7

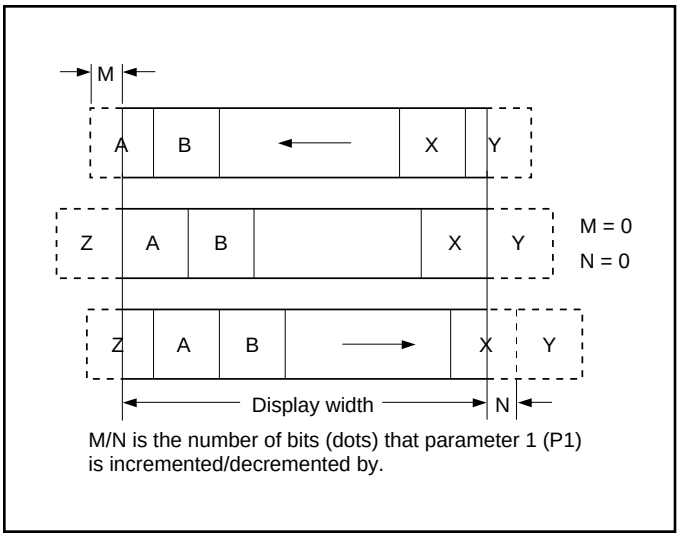


Figure 27. Horizontal scrolling

3.4 Drawing Control Commands

3.4.1 CSRW

The 16-bit cursor address register contains the display memory of the data at the cursor position as shown in Figure 28.

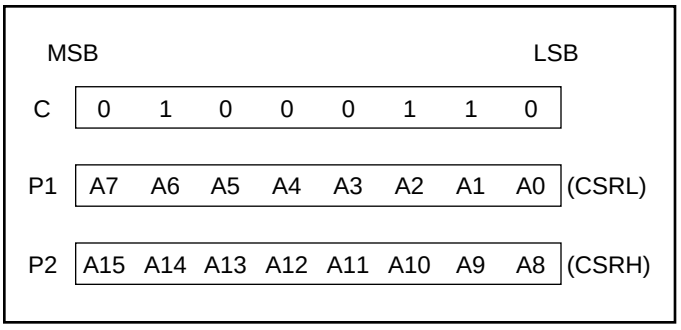


Figure 28. CSRW parameters

Note that the microprocessor cannot directly access the display memory.

The MREAD and MWRITE commands use the address in this register.

The cursor address register can only be modified by the CSRW command, and by the automatic increment after an MREAD or MWRITE command. It is not affected by display scrolling.

If a new address is not set, display memory accesses will be from the last set address or the address after previous automatic increments.

3.4.2 CSRR

Reads from the cursor address register. After issuing the command, the data read address is read twice, for the low byte and then the high byte of the register.

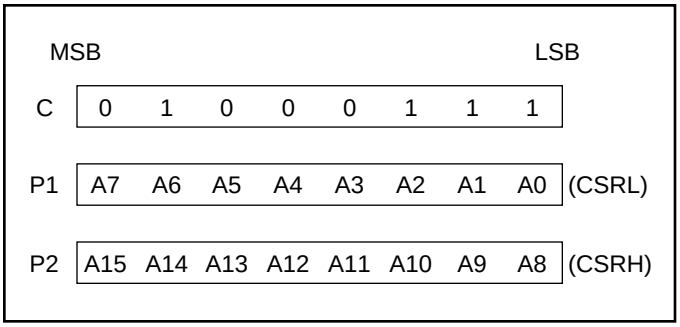


Figure 29. CSRR parameters

3.5 Memory Control Commands

3.5.1 MWRITE

The microprocessor may write a sequence of data bytes to display memory by issuing the MREAD command and then writing the bytes to the SED1330F/1335F/1336F. There is no need for further MWRITE commands or for the microprocessor to update the cursor address register after each byte as the cursor address is automatically incremented by the amount set with CSRDIR, in preparation for the next data write.

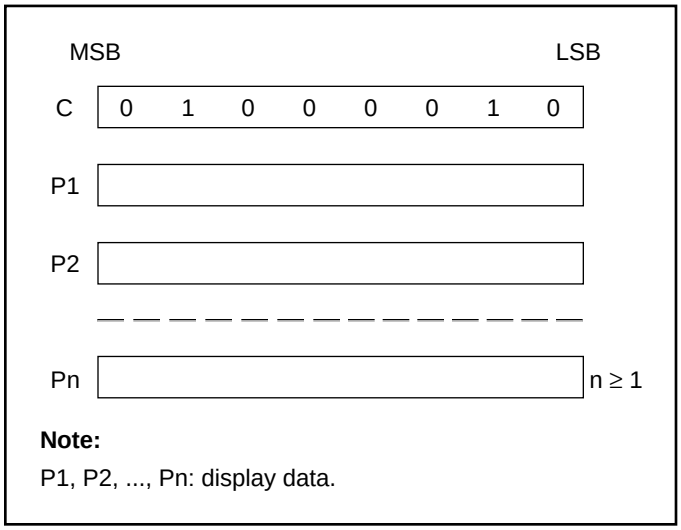


Figure 30. MWRITE parameters

3.5.2 MREAD

Puts the SED1330F/1335F/1336F into the data output state. On the MREAD command, the display memory data at the cursor address is read into a buffer in the SED1330F/1335F/1336F.

Each time the microprocessor reads the buffer, the cursor address is incremented by the amount set by CSRDIR and the next data byte fetched from memory, so a sequence of data bytes may be read without further MREAD commands or by updating the cursor address register.

If the cursor is displayed, the read data will be from two positions ahead of the cursor.

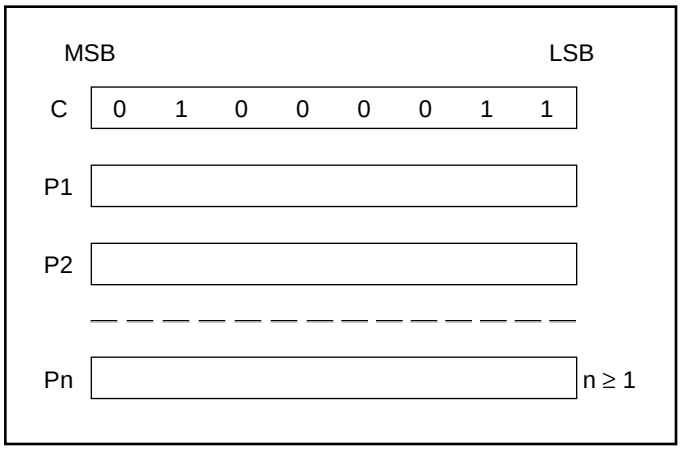


Figure 31. MREAD parameters

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4.0
Specifications

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4.0 Specifications

4.1 Absolute Maximum Ratings

4.1.1 SED1330

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.5 to V_{DD} + 0.5	V
Power dissipation	P_D	300	mW
Operating temperature range	T_{opr}	–20 to 75	°C
Storage temperature range	T_{stg}	–65 to 150	°C
Soldering temperature (10 seconds). See note 1.	T_{solder}	260	°C

4.1.2 SED1335/SED1336

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	300	mW
Operating temperature range	T_{opr}	–20 to 75	°C
Storage temperature range	T_{stg}	–65 to 150	°C
Soldering temperature (10 seconds). See note 1.	T_{solder}	260	°C

Notes:

1. The humidity resistance of the flat package may be reduced if the package is immersed in solder. Use a soldering technique that does not heatstress the package.
2. If the power supply has a high impedance, a large voltage differential can occur between the input and supply voltages. Take appropriate care with the power supply and the layout of the supply lines. (See Section 2.3.)
3. All supply voltages are referenced to V_{SS} = 0V.

4.2 SED 1330 Electrical Characteristics

V_{DD} = 5V ±10%, V_{SS} = 0V, T_a = –20 to 75°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Register data retention voltage	V_{OH}		2.0	—	5.5	V
Input leakage current	I_{LI}	$V_I = V_{DD}$.	—	0.05	2.0	µA
Output leakage current	I_{LO}	$V_I = V_{SS}$.	—	0.10	5.0	µA
Operating supply current	I_{opr}	See note 4.	—	8	12	mA
Quiescent supply current	I_Q	$V_{OSC1} = V_{\overline{CS}} = V_{\overline{RD}} = V_{DD}$	—	0.05	20.0	µA
Oscillator frequency	f_{OSC}	Measured at OSC1	1.0	—	10.0	MHz
External clock frequency	f_{CL}		—	—	10.0	MHz
Oscillator feedback resistance	R_f		0.5	1.0	5.0	MΩ
TTL						
HIGH-level input voltage	V_{IHT}	See note 1.	2.2	—	V_{DD} + 0.3	V
LOW-level input voltage	V_{ILT}	See note 1.	–0.3	—	0.8	V
HIGH-level output voltage	V_{OHT}	I_{OH} = –5.0 mA. See note 1.	2.4	—	—	V
LOW-level output voltage	V_{OLT}	I_{OL} = 5.0 mA. See note 1.	—	—	0.4	V
CMOS						
HIGH-level input voltage	V_{IHC}	See note 2.	0.8V_{DD}	—	—	V
LOW-level input voltage	V_{ILC}	See note 2.	—	—	0.2V_{DD}	V
HIGH-level output voltage	V_{OHC}	I_{OH} = –1.6 mA. See note 2.	V_{DD} – 0.4	—	—	V
LOW-level output voltage	V_{OLC}	I_{OH} = 1.6 mA. See note 2.	—	—	0.4	V
Schmitt-trigger						
Rising-edge threshold voltage	V_{T+}	See note 3.	0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V
Falling-edge threshold voltage	V_{T-}	See note 3.	0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V

Notes:

1. D0 to D7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, VD0 to VD7, VA0 to VA15, VR/$\overline{W}$ and $\overline{VCE}$ are TTL-level inputs.
2. SEL1, SEL2 and OSC1 are CMOS-level inputs. YD, XD0 to XD3, XSCL, YECL, LP, WF, YSCL, YDIS and CLO are CMOS-level outputs.
3. $\overline{RES}$ is a Schmitt-trigger input. The pulsewidth on $\overline{RES}$ must be at least 200 µs. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.
4. f_{OSC} = 10 MHz, no load (no display memory), internal character generator, 256 × 200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.

4.3 SED1335/1336 Electrical Characteristics

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, T_a = –20 to 75°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Register data retention voltage	V_{OH}		2.0	—	6.0	V
Input leakage current	I_{LI}	V_I = V_{DD}. See note 6.	—	0.05	2.0	µA
Output leakage current	I_{LO}	V_I = V_{SS}. See note 6.	—	0.10	5.0	µA
Operating supply current	I_{opr}	See note 4.	—	11	15	mA
Quiescent supply current	I_Q	Sleep mode, V_{OSC1} = $V_{\overline{CS}}$ = $V_{\overline{RD}}$ = V_{DD}	—	0.05	20.0	µA
Oscillator frequency	f_{OSC}	Measured at crystal, 47.5% duty cycle. See note 7.	1.0	—	10.0	MHz
External clock frequency	f_{CL}		1.0	—	10.0	MHz
Oscillator feedback resistance	R_f		0.5	1.0	3.0	MΩ
TTL						
HIGH-level input voltage	V_{IHT}	See note 1.	0.5V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILT}	See note 1.	V_{SS}	—	0.2V_{DD}	V
HIGH-level output voltage	V_{OHT}	I_{OH} = –5.0 mA. See note 1.	2.4	—	—	V
LOW-level output voltage	V_{OLT}	I_{OL} = 5.0 mA. See note 1.	—	—	V_{SS} + 0.4	V
CMOS						
HIGH-level input voltage	V_{IHC}	See note 2.	0.8V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILC}	See note 2.	V_{SS}	—	0.2V_{DD}	V
HIGH-level output voltage	V_{OHC}	I_{OH} = –2.0 mA. See note 2.	V_{DD} – 0.4	—	—	V
LOW-level output voltage	V_{OLC}	I_{OH} = 1.6 mA. See note 2.	—	—	V_{SS} + 0.4	V
Open-drain						
LOW-level output voltage	V_{OLN}	I_{OL} = 6.0 mA. See note 5.	—	—	V_{SS} + 0.4	V
Schmitt-trigger						
Rising-edge threshold voltage	V_{T+}	See note 3.	0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V
Falling-edge threshold voltage	V_{T-}	See note 3.	0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V

Notes:

1. D0 to D7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, VD0 to VD7, VA0 to VA15, $\overline{VRD}$, $\overline{VWR}$ and $\overline{VCE}$ are TTL-level inputs.
2. SEL1 and NT/PL are CMOS-level inputs. YD, XD0 to XD3, XSCL, XECL, LP, WF, YSCL, YDIS and CLO are CMOS-level outputs.
3. $\overline{RES}$ is a Schmitt-trigger input. The pulsewidth on $\overline{RES}$ must be at least 200 µs. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.
4. f_{OSC} = 10 MHz, no load (no display memory), internal character generator, 256 × 200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.

4.4 SED1330 Timing Diagrams

4.4.1 System bus READ/WRITE timing I (8080)

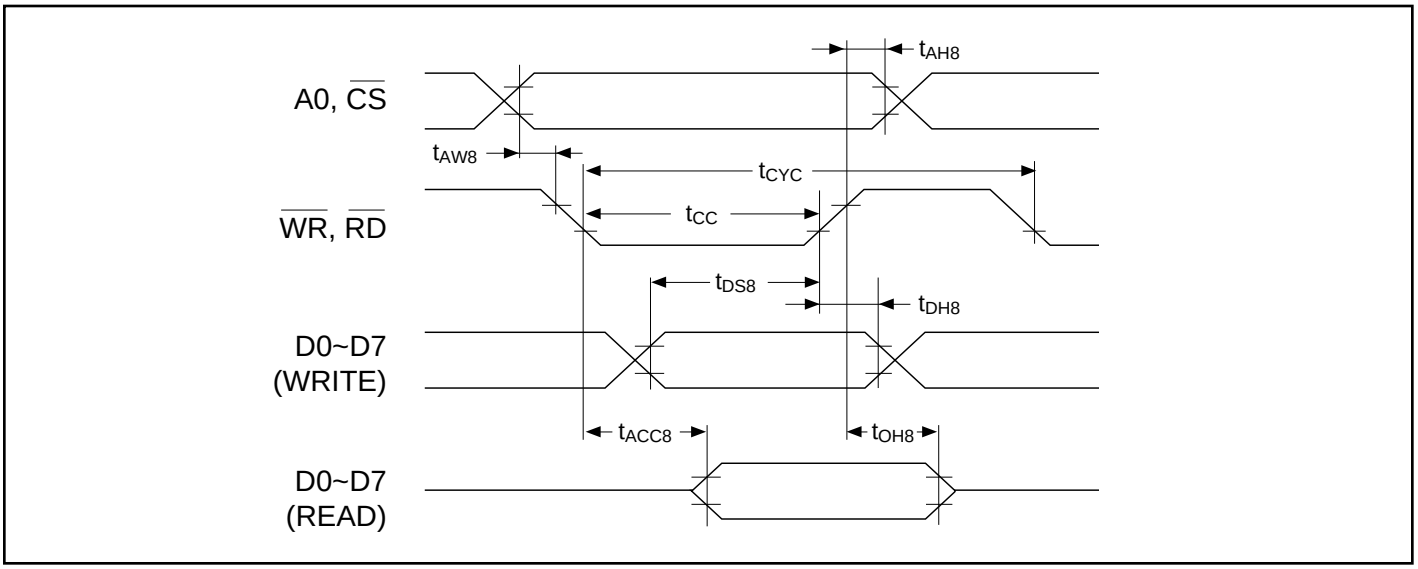


Figure 32. System bus READ/WRITE timing I (8080)

4.4.1.1 SED1330F

Ta = –20 to 75°C

Signal	Symbol	Parameter	Rating		Unit	Condition
			min	max		
A0, CS	tAH8	Address hold time	10	—	ns	CL = 100 pF
	tAW8	Address setup time	30	—	ns	
WR, RD	tCYC	System cycle time	(1)	—	ns	
	tCC	Strobe pulsewidth	220	—	ns	
D0 to D7	tDS8	Data setup time	120	—	ns	
	tDH8	Data hold time	10	—	ns	
	tACC8	RD access time	—	120	ns	
	tOH8	Output disable time	10	50	ns	

Note: t_{CYC} = $2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$:
memory control/movement control commands:
$= 4t_C + t_{CC} + 30$:
all other commands:

4.4 SED1330 Timing Diagrams

4.4.2 System bus READ/WRITE timing II (6800)

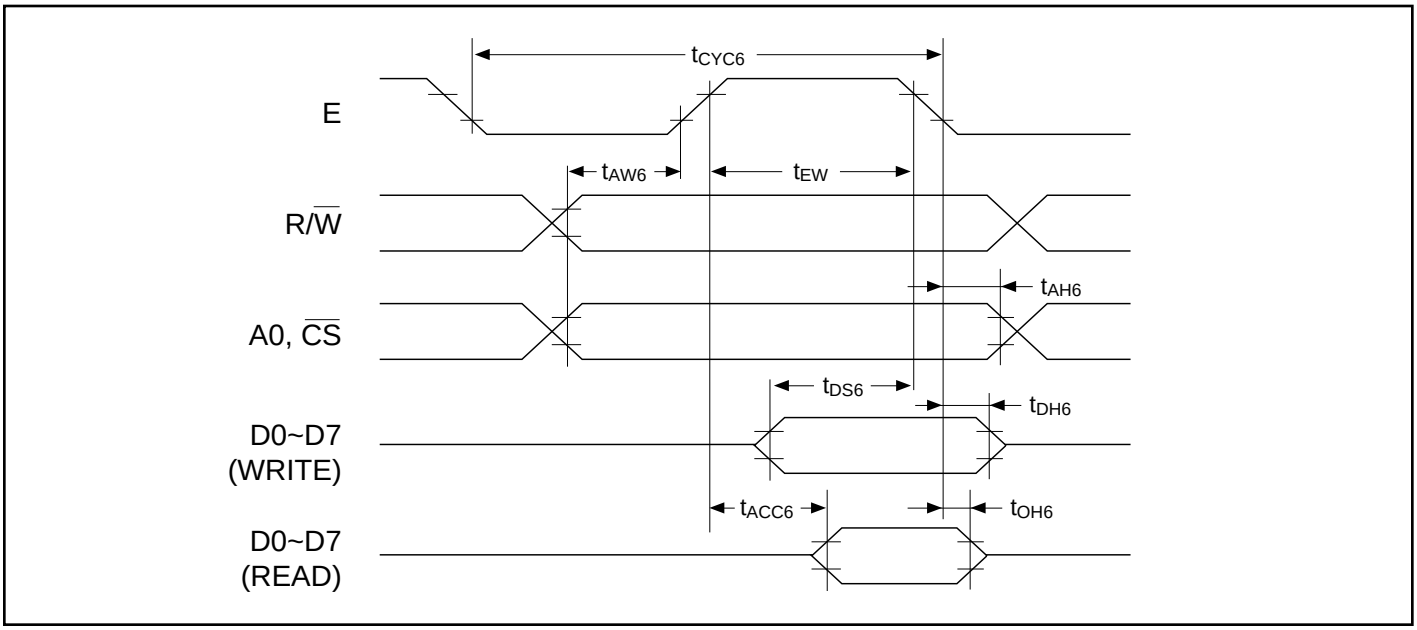


Figure 33. System bus READ/WRITE timing II (6800)

4.4.2.1 SED1330F

T_a = –20 to 75°C

Signal	Symbol	Parameter	Rating		Unit	Condition
			min	max		
A0, $\overline{CS}$ R/$\overline{W}$	t_{AH6}	Address hold time	10	—	ns	CL=100pF+1TTL pF
	t_{AW6}	Address setup time	30	—	ns	
	t_{CYC6}	System cycle time	(1)	—	ns	
D0 to D7	t_{DS6}	Data setup time	120	—	ns	
	t_{DH6}	Data hold time	10	—	ns	
	t_{ACC6}	Access time	—	120	ns	
	t_{OH6}	Output disable time	10	50	ns	
E	t_{EW}	Enable pulse width	220	—	ns	

Note: (1) t_{CYC6} = $2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$:
memory control/movement control commands:
$= 4t_C + t_{EW} + 30$:
all other commands:

1. t_{CYC6} means a cycle of ($\overline{CS}$.E) not E alone.

4.4 SED1330 Timing Diagrams

4.4.3 Display memory READ timing

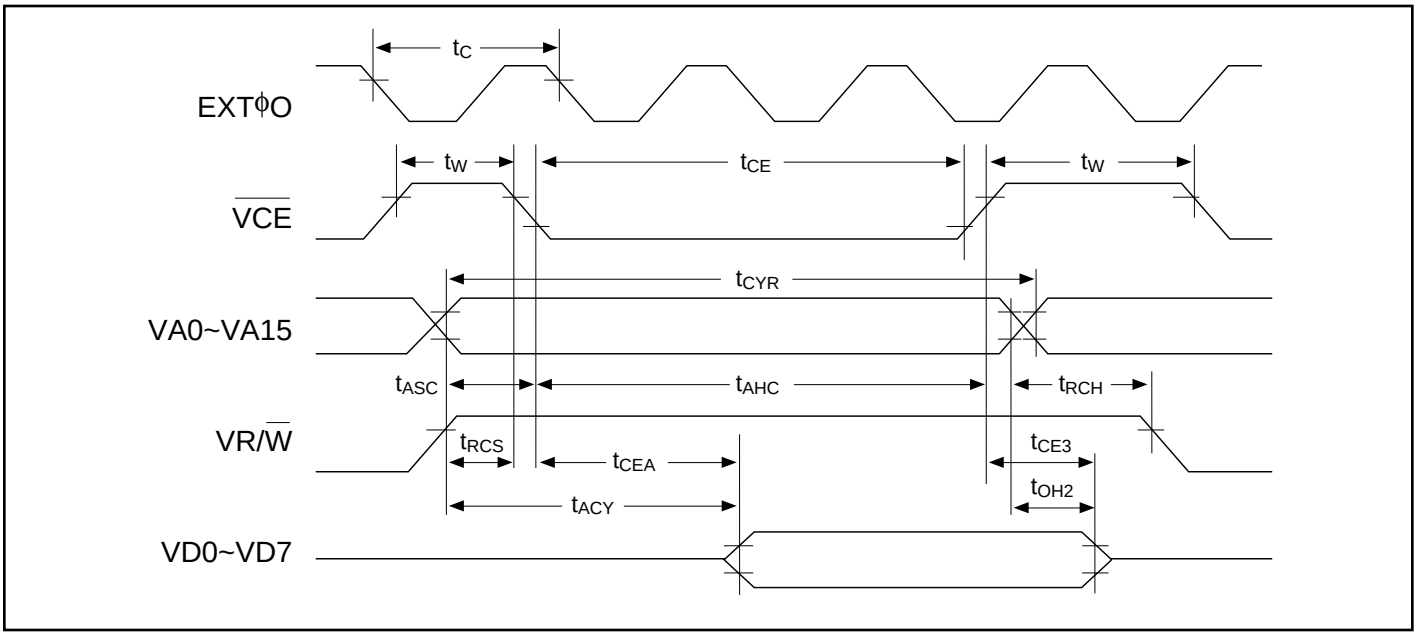


Figure 34. Display memory READ timing

4.4.3.1 SED1330F

Ta = –20 to 75°C

Signal	Symbol	Parameter	Rating		Unit	Condition
			min	max		
EXT ø0	tC	Clock cycle	100	—	ns	CL = 100pF +1TTL
$\overline{VCE}$	tW	$\overline{VCE}$ high level pulse width	tc–40	—	ns	
	tCE	$\overline{VCE}$ low level pulse width	2tc–40	—	ns	
VA0 to VA15	tCYR	Read cycle time	(1)	—	ns	
	tASC	$\overline{VCE}$ address setup time (fall)	tc–45	—	ns	
	tAHC	$\overline{VCE}$ address hold time (fall)	2tc–40	—	ns	
VR/$\overline{W}$	tRCS	$\overline{VCE}$ read cycle setup time (fall)	tc–45	—	ns	
	tRCH	$\overline{VCE}$ read cycle hold time (fall)	tc/2–35	—	ns	
VD0 to VD7	tACV	Address access time	—	(2)	ns	
	tCEA	$\overline{VCE}$ access time	—	(3)	ns	
	tOH2	Output data hold time	0	—	ns	
	tCE2	$\overline{VCE}$ data off time	0	—	ns	

Note: 1. $t_{CYR} = 3t_C$
2. $t_{ACV} = 3t_C - 120$
3. $t_{CEA} = 2t_C - 120$

4.4 SED1330 Timing Diagrams

4.4.4 Display memory WRITE timing

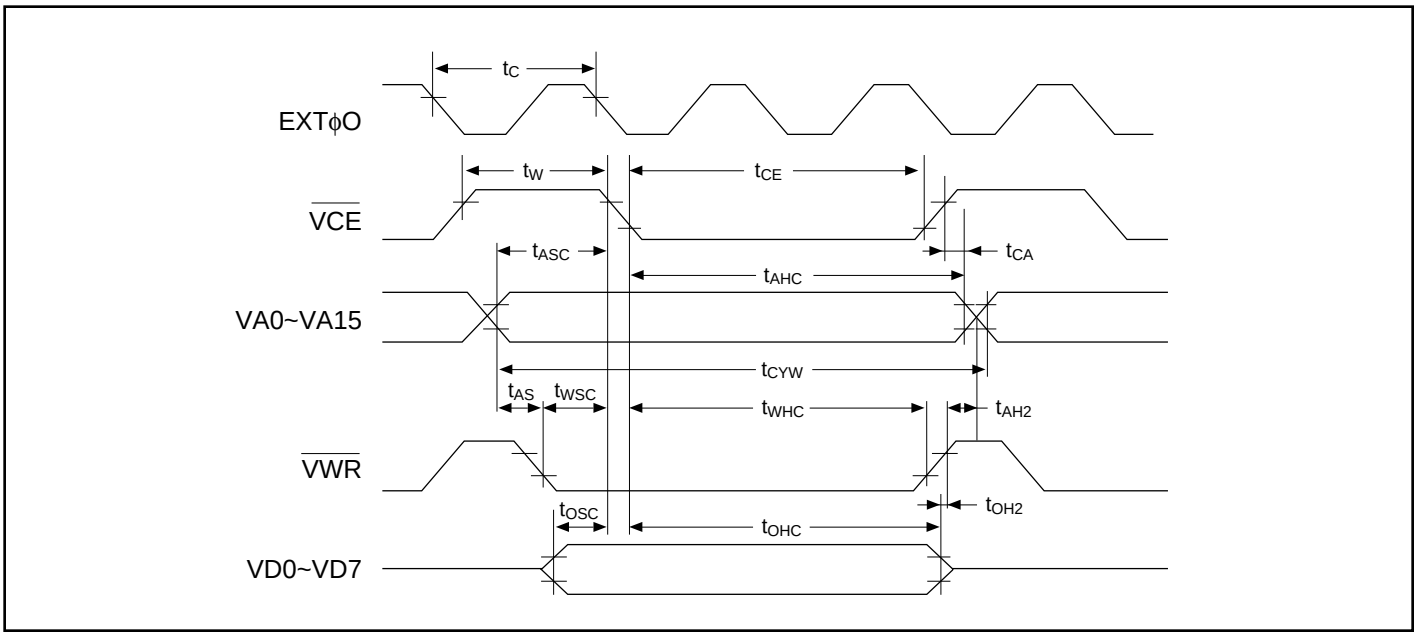


Figure 35. Display memory WRITE timing

4.4.4.1 SED1330F

Ta = –20 to 75°C

Signal	Symbol	Parameter	Rating		Unit	Condition
			min	max		
EXT ø0	tC	Clock cycle	100	—	ns	CL = 100pF +1TTL
$\overline{VCE}$	tW	$\overline{VCE}$ high level pulse width	tc–40	—	ns	
	tCE	$\overline{VCE}$ low level pulse width	2tc–40	—	ns	
VA0 to VA15	tCYW	Write cycle time	3tc	—	ns	
	tAHC	$\overline{VCE}$ address hold time (fall)	2tc–40	—	ns	
	tASC	$\overline{VCE}$ address setup time (fall)	tc–55	—	ns	
	tCA	$\overline{VCE}$ address hold time (rise)	5	—	ns	
	tAS	VR/$\overline{W}$ address setup time (fall)	0	—	ns	
	tAH2	VR/$\overline{W}$ address hold time (rise)	15	—	ns	
VR/$\overline{W}$	tWSC	$\overline{VCE}$ write setup time (fall)	tc–55	—	ns	
	tWHC	$\overline{VCE}$ write hold time (fall)	tc2–40	—	ns	
VD0 to VD7	tDSC	$\overline{VCE}$ data input setup time (fall)	twsc–10	—	ns	
	tDHC	$\overline{VCE}$ data input hold time (fall)	2tc–30	—	ns	
	tDH2	VR/$\overline{W}$ data hold time (rise)	10*	50	ns	

* Lines VD0 to VD7 are latched.

4.4 SED1330 Timing Diagrams

4.4.5 LCD control timing

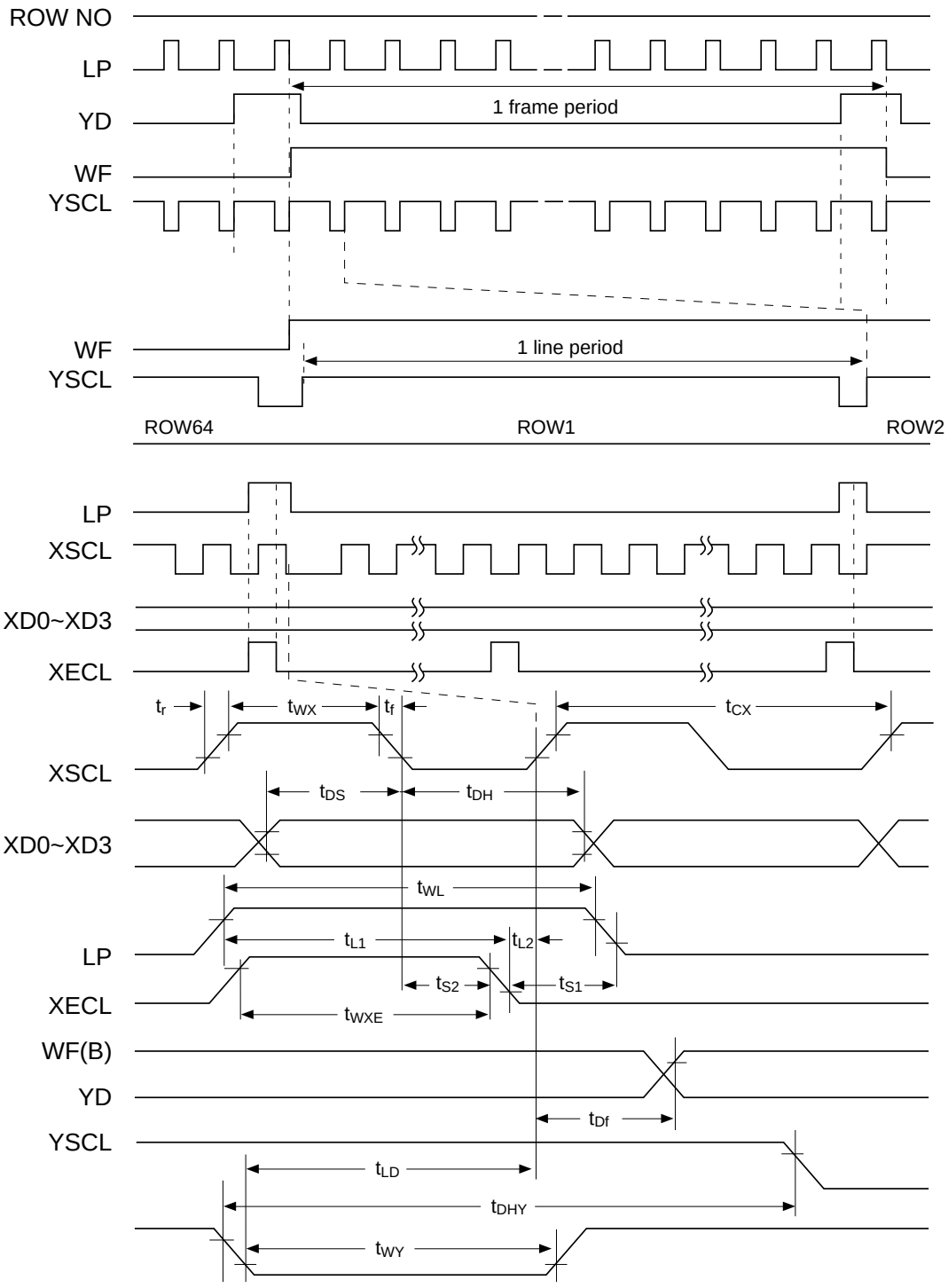


Figure 36. LCD control timing

4.4 SED1330 Timing Diagrams

4.4.5.1 SED1330F

T_a = –20 to 75°C

Signal	Symbol	Parameter	Rating		Unit	Condition
			min	max		
EXT ø0	t_C	Clock cycle	100	—	ns	V_{DD} = 5.0V ±10% CL=150F
	t_r	$\overline{VCE}$ high level pulse width	—	35	ns	
	t_f	$\overline{VCE}$ low level pulse width	—	35	ns	
XSCL	t_{CX}	Shift clock cycle time	4tc	—	ns	
	t_{WX}	XSCL clock pulse width	t_{CX2}–80	—	ns	
XD0 to XD3	t_{DH}	X-data hold time	t_{CX2}–100	—	ns	
	t_{DS}	X-data setup time	t_{CX2}–100	—	ns	
LP	t_{LS}	Latch data setup time	t_{CX2}–100	—	ns	
	t_{WL}	LP signal pulse width	t_{CX4}–80	—	ns	
XECL	t_{L1}	XECL setup time	t_{CX3}–100	—	ns	
	t_{L2}	XECL data hold time	t_C–30	—	ns	
	t_{S1}	Enable setup time	t_C–30	—	ns	
	t_{S1}	Enable delay time	t_C–30	—	ns	
	t_{WXE}	XECL clock pulse width	t_{CX3}–80	—	ns	
WF	t_{DF}	Time allowance of WF delay	—	100	ns	
YSCL	t_{LD}	LP delay time against YSCL	t_{CX4}–100	—	ns	
	t_{WY}	YSCL clock pulse width	t_{CX4}–80	—	ns	
YD	t_{DHY}	Y-data hold time	t_{CX6}–100	—	ns	

4.4 SED1330 Timing Diagrams

4.4.6 Oscillator timing

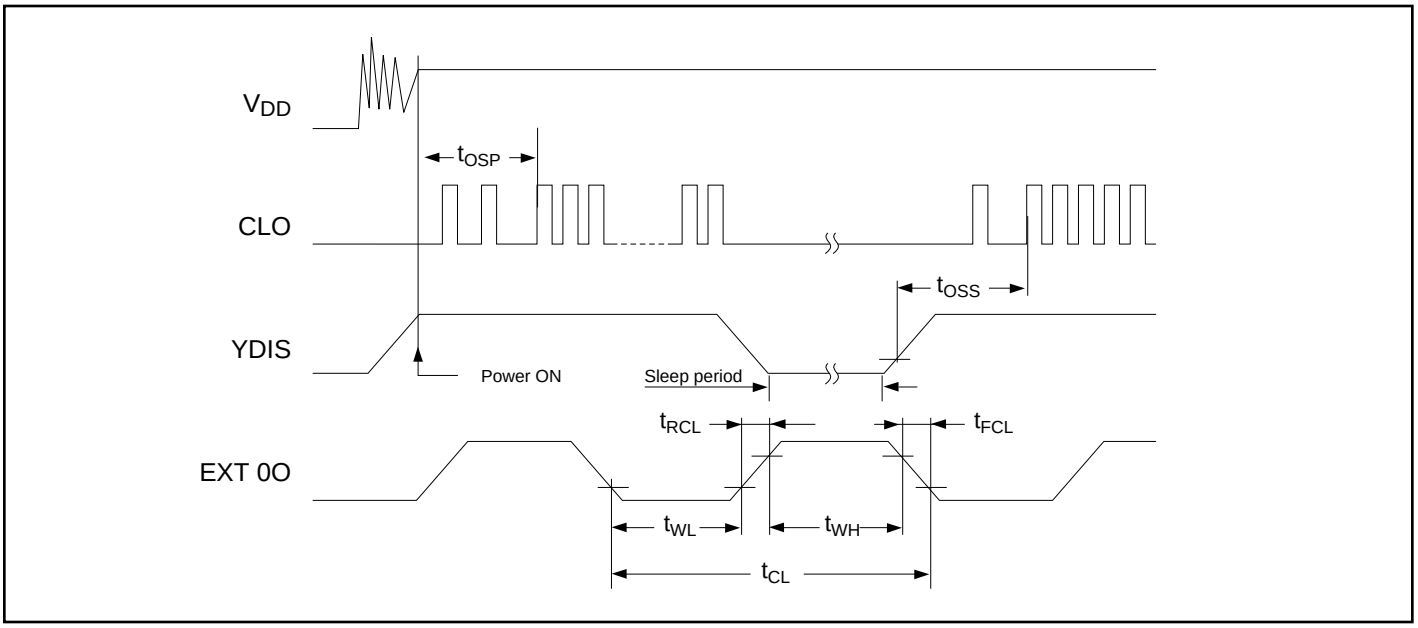


Figure 37. Oscillator timing

4.4.6.1 SED1330F

Ta = –20 to 75°C

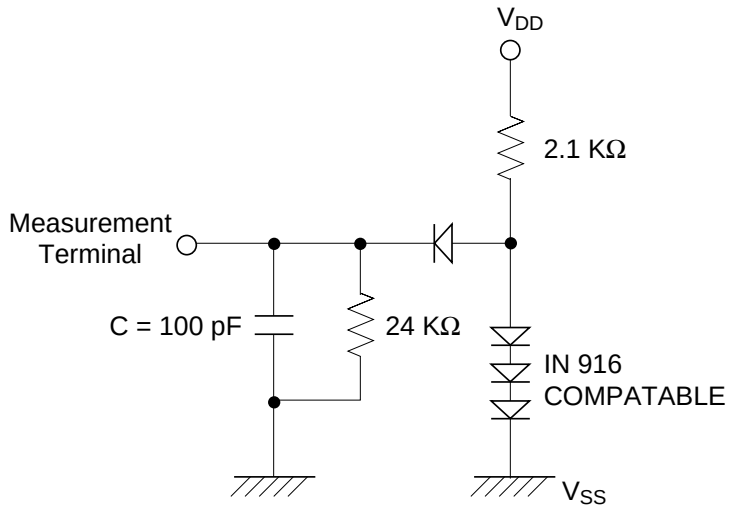
Signal	Symbol	Parameter	Rating		Unit	Condition
			min	max		
CLO	tOSP	Time to stable CLO output after power ON	—	3	ms	$\overline{RES}$ = H
	tOSS	Time to stable CLO output after sleep OFF	—	1	ms	20 pF
EXTø0	tRCL	External clock rise time	—	15	ns	
	tFCL	External clock fall time	—	15	ns	
	tWH	External clock high-pulse width	Note 1	Note 2	ns	
	tWL	External clock low-pulse width	Note 1	Note 2	ns	
	tCL	External clock cycle	100	—	ns	

1. $(t_C - t_{RCL} - t_{FCL}) \times 475/1000 < t_{WH}, t_{WL}$

2. $(t_C - t_{RCL} - t_{FCL}) \times 525/1000 > t_{WH}, t_{WL}$

4.4 SED1330 Timing Diagrams

4.4.7 Measurement circuit



* C includes probe capacitance.

Figure 38. Measurement circuit

4.5 SED1335/SED1336 AC Timing Diagrams

4.5.1 8080 family Interface Timing

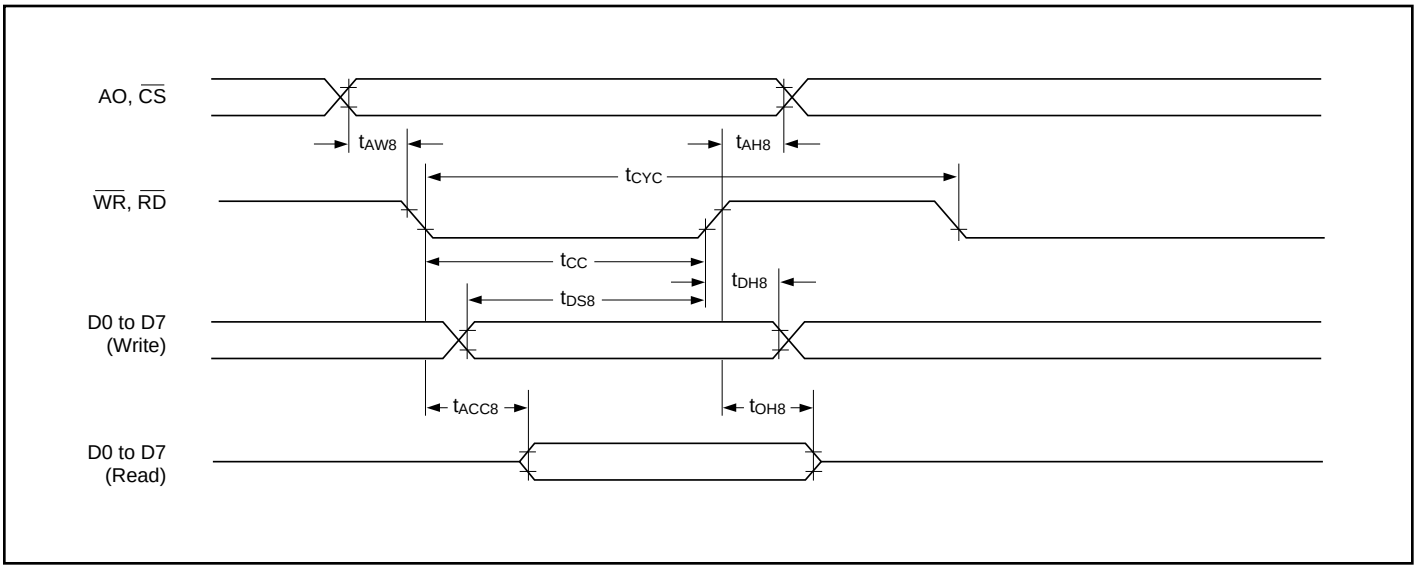


Figure 39. 8080 family interface timing

4.5.1.1 SED1335F

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
A0, CS	t_{AH8}	Address hold time	10	—	10	—	ns	CL = 100 pF
	t_{AW8}	Address setup time	0	—	0	—	ns	
WR, RD	t_{CYC}	System cycle time	See note	—	See note	—	ns	
	t_{CC}	Strobe pulsewidth	120	—	150	—	ns	
D0 to D7	t_{DS8}	Data setup time	120	—	120	—	ns	
	t_{DH8}	Data hold time	5	—	5	—	ns	
	t_{ACC8}	RD access time	—	50	—	80	ns	
	t_{OH8}	Output disable time	10	50	10	55	ns	

Note: For memory control and system control commands:

$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4t_C + t_{CC} + 30$

4.5.1.2 SED1336F

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
A0, $\overline{CS}$	t_{AH8}	Address hold time	10	—	10	—	ns	CL = 100 pF
	t_{AW8}	Address setup time	0	—	0	—	ns	
$\overline{WR}$, $\overline{RD}$	t_{CYC}	System cycle time	See note	—	See note	—	ns	
	t_{CC}	Strobe pulsewidth	120	—	140	—	ns	
D0 to D7	t_{DS8}	Data setup time	120	—	120	—	ns	
	t_{DH8}	Data hold time	5	—	5	—	ns	
	t_{ACC8}	$\overline{RD}$ access time	—	50	—	70	ns	
	t_{OH8}	Output disable time	10	50	10	50	ns	

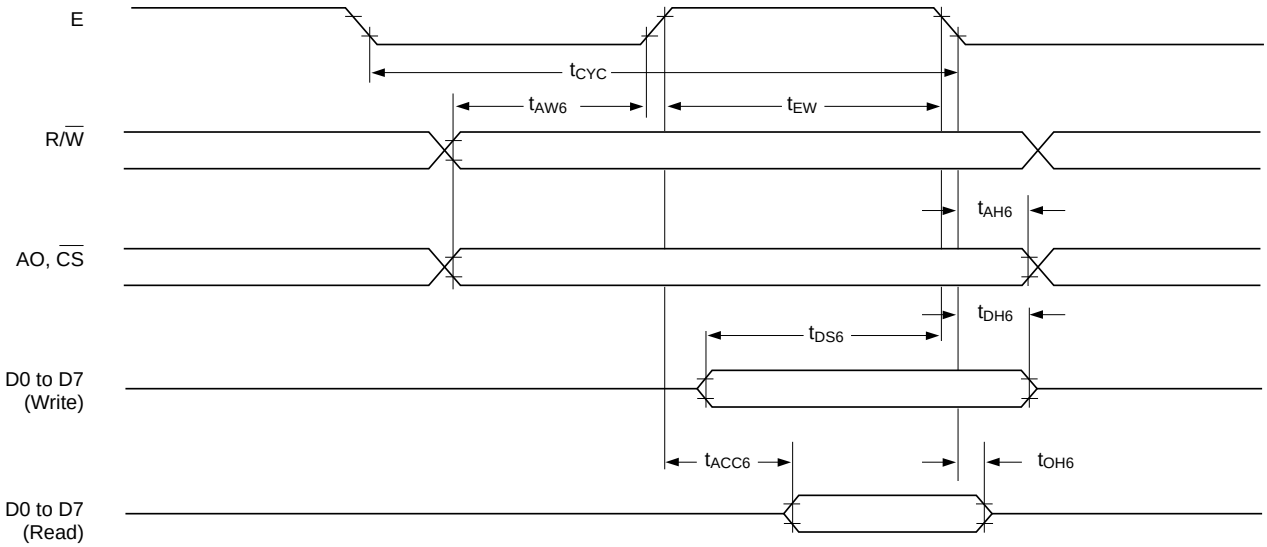
Note: For memory control and system control commands:

$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4t_C + t_{CC} + 30$

4.5.2 6800 family Interface Timing



Note: t_{CYC6} indicates the interval during which CS is LOW and E is HIGH.

Figure 40. 6800 family interface timing

4.5.2.1 SED1335F

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
A0, $\overline{CS}$, R/$\overline{W}$	t_{CYC6}	System cycle time	See note	—	See note	—	ns	CL = 100 pF
	t_{AW6}	Address setup time	0	—	10	—	ns	
	t_{AH6}	Address hold time	0	—	0	—	ns	
D0 to D7	t_{DS6}	Data setup time	100	—	120	—	ns	
	t_{DH6}	Data hold time	0	—	0	—	ns	
	t_{OH6}	Output disable time	10	50	10	75	ns	
	t_{ACC6}	Access time	—	85	—	130	ns	
E	t_{EW}	Enable pulsewidth	120	—	150	—	ns	

Note: For memory control and system control commands:

$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC6} = 4t_C + t_{EW} + 30$

4.5.2.2 SED1336F

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
A0, $\overline{CS}$, R/$\overline{W}$	t_{CYC6}	System cycle time	See note	—	See note	—	ns	CL = 100 pF
	t_{AW6}	Address setup time	0	—	10	—	ns	
	t_{AH6}	Address hold time	0	—	0	—	ns	
D0 to D7	t_{DS6}	Data setup time	100	—	120	—	ns	
	t_{DH6}	Data hold time	0	—	0	—	ns	
	t_{OH6}	Output disable time	10	50	10	70	ns	
	t_{ACC6}	Access time	—	85	—	120	ns	
E	t_{EW}	Enable pulsewidth	120	—	140	—	ns	

Note: For memory control and system control commands:

$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC6} = 4t_C + t_{EW} + 30$

4.5.3 Display Memory Read Timing

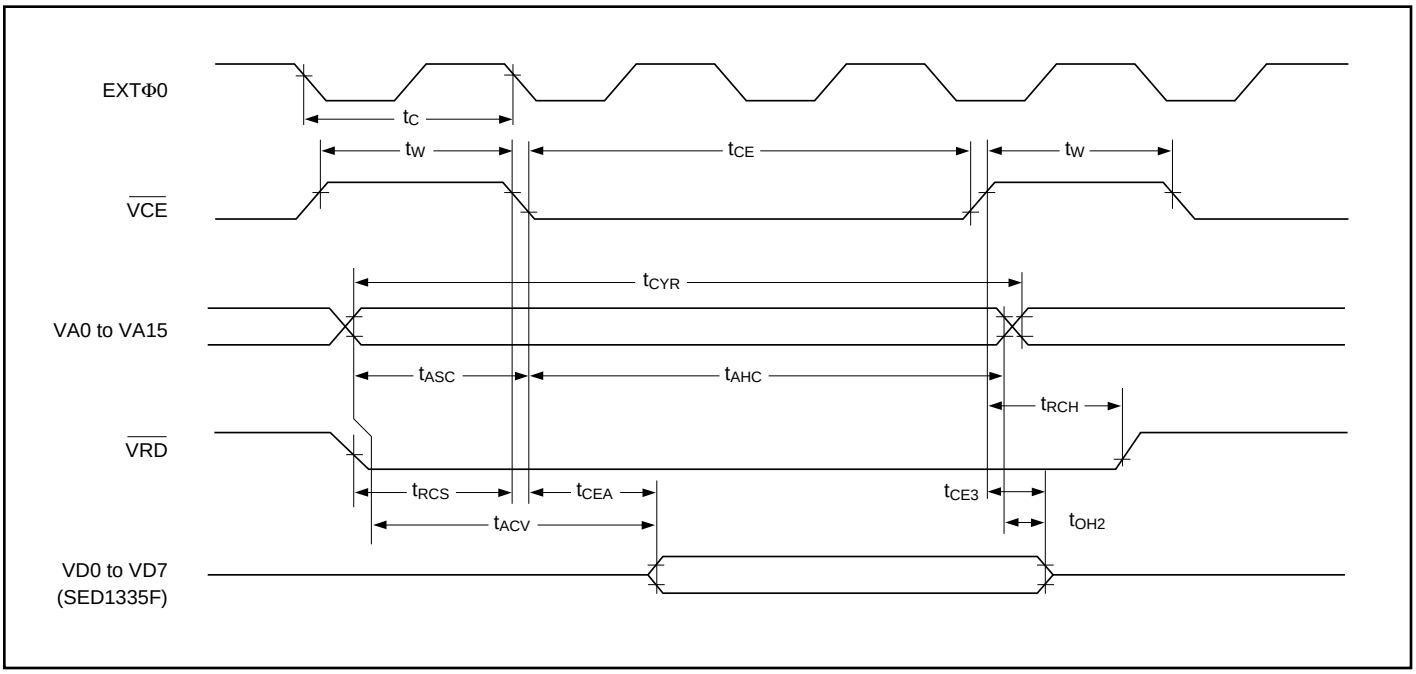


Figure 41. Display memory read timing

4.5.3.1 SED1335F

Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	tC	Clock period	100	—	125	—	ns	CL = 100 pF
VCE	tW	VCE HIGH-level pulse-width	tC – 50	—	tC – 50	—	ns	
	tCE	VCE LOW-level pulse-width	2tC – 30	—	2tC – 30	—	ns	
VA0 to VA15	tCYR	Read cycle time	3tC	—	3tC	—	ns	
	tASC	Address setup time to falling edge of VCE	tC – 70	—	tC – 100	—	ns	
	tAHC	Address hold time from falling edge of VCE	2tC – 30	—	2tC – 40	—	ns	
VRD	tRCS	Read cycle setup time to falling edge of VCE	tC – 45	—	tC – 60	—	ns	
	tRCH	Read cycle hold time from rising edge of VCE	0.5tC	—	0.5tC	—	ns	
VD0 to VD7	tACV	Address access time	—	3tC – 100	—	3tC – 115	ns	
	tCEA	VCE access time	—	2tC – 80	—	2tC – 90	ns	
	tOH2	Output data hold time	0	—	0	—	ns	
	tCE3	VCE to data off time	0	—	0	—	ns	

4.5.3.2 SED1336F

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	t_C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	t_W	$\overline{VCE}$ HIGH-level pulse-width	t_C – 50	—	t_C – 50	—	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulse-width	2t_C – 30	—	2t_C – 30	—	ns	
VA0 to VA15	t_{CYR}	Read cycle time	3t_C	—	3t_C	—	ns	
	t_{ASC}	Address setup time to falling edge of $\overline{VCE}$	t_C – 70	—	t_C – 100	—	ns	
	t_{AHC}	Address hold time from falling edge of $\overline{VCE}$	2t_C – 30	—	2t_C – 40	—	ns	
$\overline{VRD}$	t_{RCS}	Read cycle setup time to falling edge of $\overline{VCE}$	t_C – 45	—	t_C – 55	—	ns	
	t_{RCH}	Read cycle hold time from rising egde of $\overline{VCE}$	0.5t_C	—	0.5t_C	—	ns	
VD0 to VD7	t_{ACV}	Address access time	—	3t_C – 100	—	3t_C – 110	ns	
	t_{CEA}	$\overline{VCE}$ access time	—	2t_C – 80	—	2t_C – 85	ns	
	t_{OH2}	Output data hold time	0	—	0	—	ns	
	t_{CE3}	$\overline{VCE}$ to data off time	0	—	0	—	ns	

4.5.4 Display Memory Write Timing

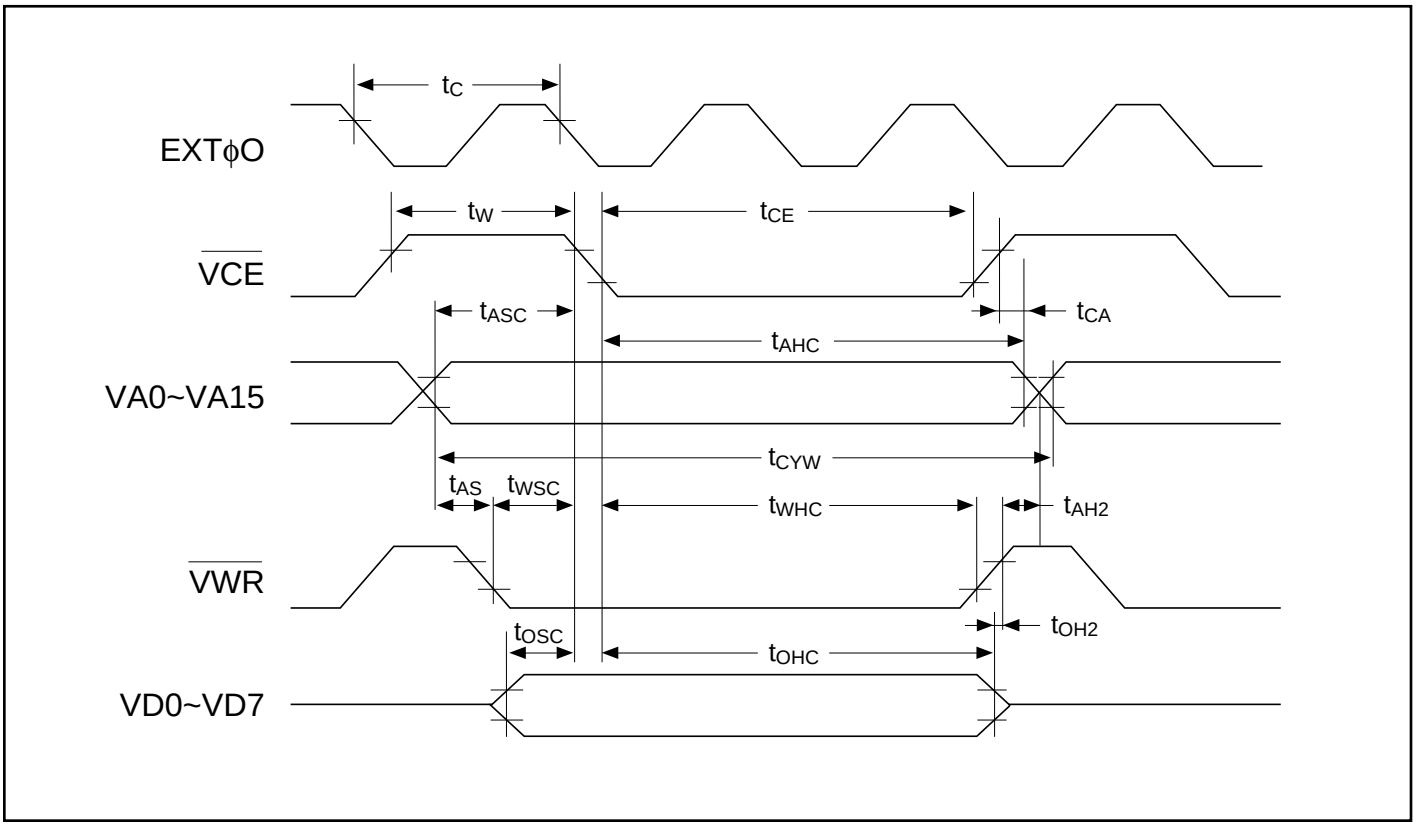


Figure 42. Display memory write timing

4.5.4.1 SED1335F

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	t_C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	t_W	$\overline{VCE}$ HIGH-level pulse-width	t_C – 50	—	t_C – 50	—	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulse-width	2t_C – 30	—	2t_C – 30	—	ns	
VA0 to VA15	t_{CYW}	Write cycle time	3t_C	—	3t_C	—	ns	
	t_{AHC}	Address hold time from falling edge of $\overline{VCE}$	2t_C – 30	—	2t_C – 40	—	ns	
	t_{ASC}	Address setup time to falling edge of $\overline{VCE}$	t_C – 70	—	t_C – 110	—	ns	
	t_{CA}	Address hold time from rising edge of $\overline{VCE}$	0	—	0	—	ns	
	t_{AS}	Address setup time to falling edge of $\overline{VWR}$	0	—	0	—	ns	
	t_{AH2}	Address hold time from rising edge of $\overline{VWR}$	10	—	10	—	ns	
$\overline{VWR}$	t_{WSC}	Write setup time to falling edge of $\overline{VCE}$	t_C – 80	—	t_C – 115	—	ns	
	t_{WHC}	Write hold time from falling edge of $\overline{VCE}$	2t_C – 20	—	2t_C – 20	—	ns	
VD0 to VD7	t_{DSC}	Data input setup time to falling edge of $\overline{VCE}$	t_C – 85	—	t_C – 125	—	ns	
	t_{DHC}	Data input hold time from falling edge of $\overline{VCE}$	2t_C – 30	—	2t_C – 30	—	ns	
	t_{DH2}	Data hold time from rising edge of $\overline{VWR}$	5	50	5	50	ns	

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

4.5.4.2 SED1336F

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	t_C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	t_W	$\overline{VCE}$ HIGH-level pulse-width	t_C – 50	—	t_C – 50	—	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulse-width	2t_C – 30	—	2t_C – 30	—	ns	
VA0 to VA15	t_{CYW}	Write cycle time	3t_C	—	3t_C	—	ns	
	t_{AHC}	Address hold time from falling edge of $\overline{VCE}$	2t_C – 30	—	2t_C – 40	—	ns	
	t_{ASC}	Address setup time to falling edge of $\overline{VCE}$	t_C – 70	—	t_C – 100	—	ns	
	t_{CA}	Address hold time from rising edge of $\overline{VCE}$	0	—	0	—	ns	
	t_{AS}	Address setup time to falling edge of $\overline{VWR}$	0	—	0	—	ns	
	t_{AH2}	Address hold time from rising edge of $\overline{VWR}$	10	—	10	—	ns	
$\overline{VWR}$	t_{WSC}	Write setup time to falling edge of $\overline{VCE}$	t_C – 80	—	t_C – 110	—	ns	
	t_{WHC}	Write hold time from falling edge of $\overline{VCE}$	2t_C – 20	—	2t_C – 20	—	ns	
VD0 to VD7	t_{DSC}	Data input setup time to falling edge of $\overline{VCE}$	t_C – 85	—	t_C – 120	—	ns	
	t_{DHC}	Data input hold time from falling edge of $\overline{VCE}$	2t_C – 30	—	2t_C – 30	—	ns	
	t_{DH2}	Data hold time from rising edge of $\overline{VWR}$	5	50	5	50	ns	

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

4.5.5 SLEEP IN Command Timing

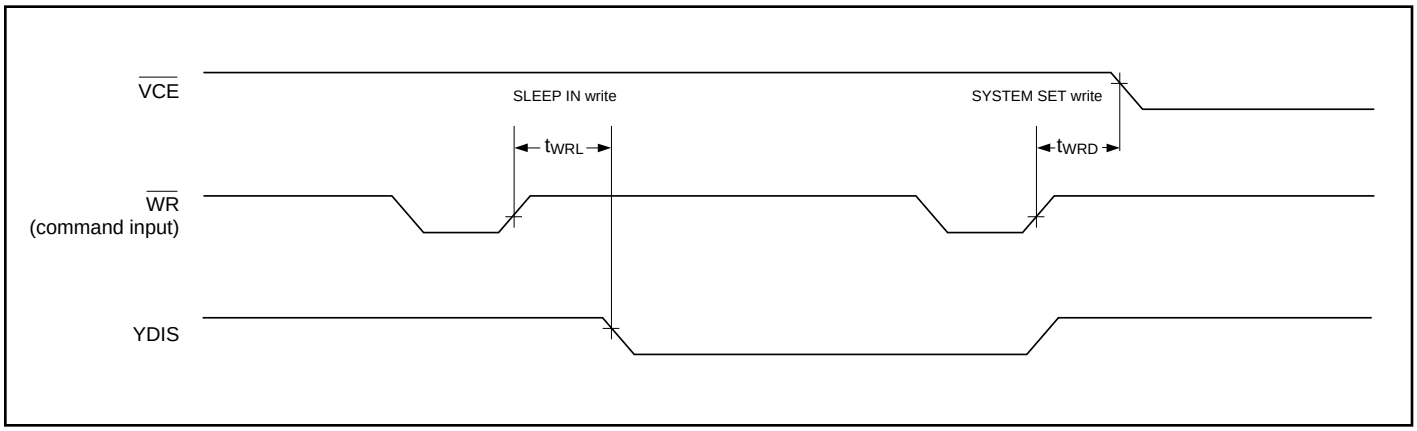


Figure 43. SLEEP IN command timing

4.5.5.1 SED1335F

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
$\overline{WR}$	t_{WRD}	$\overline{VCE}$ falling-edge delay time	See note 1	—	See note 1	—	ns	CL = 100 pF
	t_{WRL}	YDIS falling-edge delay time	—	See note 2	—	See note 2	ns	

Notes:

1. $t_{WRD} = 18t_C + t_{OSS} + 40$ (t_{OSS} is the time delay from the sleep state until stable operation)
2. $t_{WRL} = 36t_C \times [TC/R] \times [L/F] + 70$

4.5.5.2 SED1336F

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
$\overline{WR}$	t_{WRD}	$\overline{VCE}$ falling-edge delay time	See note 1	—	See note 1	—	ns	CL = 100 pF
	t_{WRL}	YDIS falling-edge delay time	—	See note 2	—	See note 2	ns	

Notes:

1. $t_{WRD} = 18t_C + t_{OSS} + 40$ (t_{OSS} is the time delay from the sleep state until stable operation)
2. $t_{WRL} = 36t_C \times [TC/R] \times [L/F] + 70$

4.5.6 External Oscillator Signal Timing

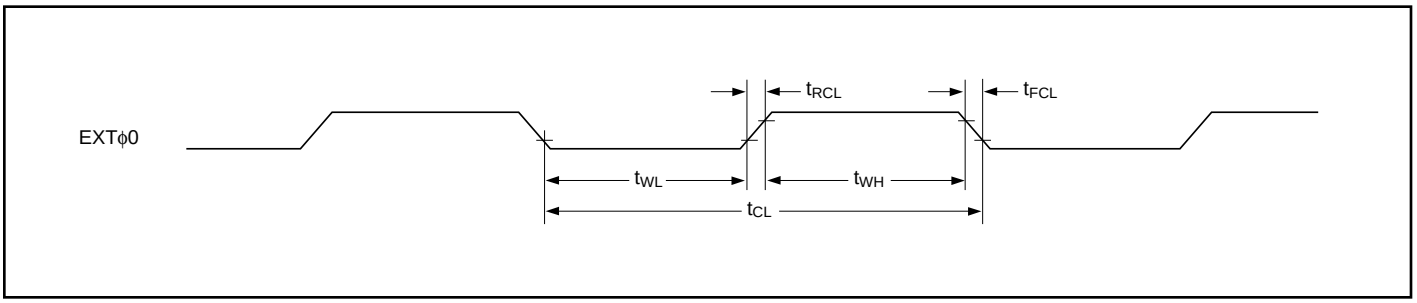


Figure 44. External oscillator signal timing

4.5.6.1 SED1335F

Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	tRCL	External clock rise time	—	15	—	15	ns	
	tFCL	External clock fall time	—	15	—	15	ns	
	tWH	External clock HIGH-level pulsewidth	See note 1	See note 2	See note 1	See note 2	ns	
	tWL	External clock LOW-level pulsewidth	See note 1	See note 2	See note 1	See note 2	ns	
	tC	External clock period	100	—	125	—	ns	

Notes:

1. $(t_C - t_{RCL} - t_{FCL}) \times \frac{475}{1000} < t_{WH}, t_{WL}$
2. $(t_C - t_{RCL} - t_{FCL}) \times \frac{525}{1000} > t_{WH}, t_{WL}$

4.5.6.2 SED1336F

Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	tRCL	External clock rise time	—	15	—	15	ns	
	tFCL	External clock fall time	—	15	—	15	ns	
	tWH	External clock HIGH-level pulsewidth	See note 1	See note 2	See note 1	See note 2	ns	
	tWL	External clock LOW-level pulsewidth	See note 1	See note 2	See note 1	See note 2	ns	
	tC	External clock period	100	—	125	—	ns	

Notes:

1. $(t_C - t_{RCL} - t_{FCL}) \times \frac{475}{1000} < t_{WH}, t_{WL}$
2. $(t_C - t_{RCL} - t_{FCL}) \times \frac{525}{1000} > t_{WH}, t_{WL}$

4.5.7 LCD Output Timing

The following characteristics are for a 1/64 duty cycle.

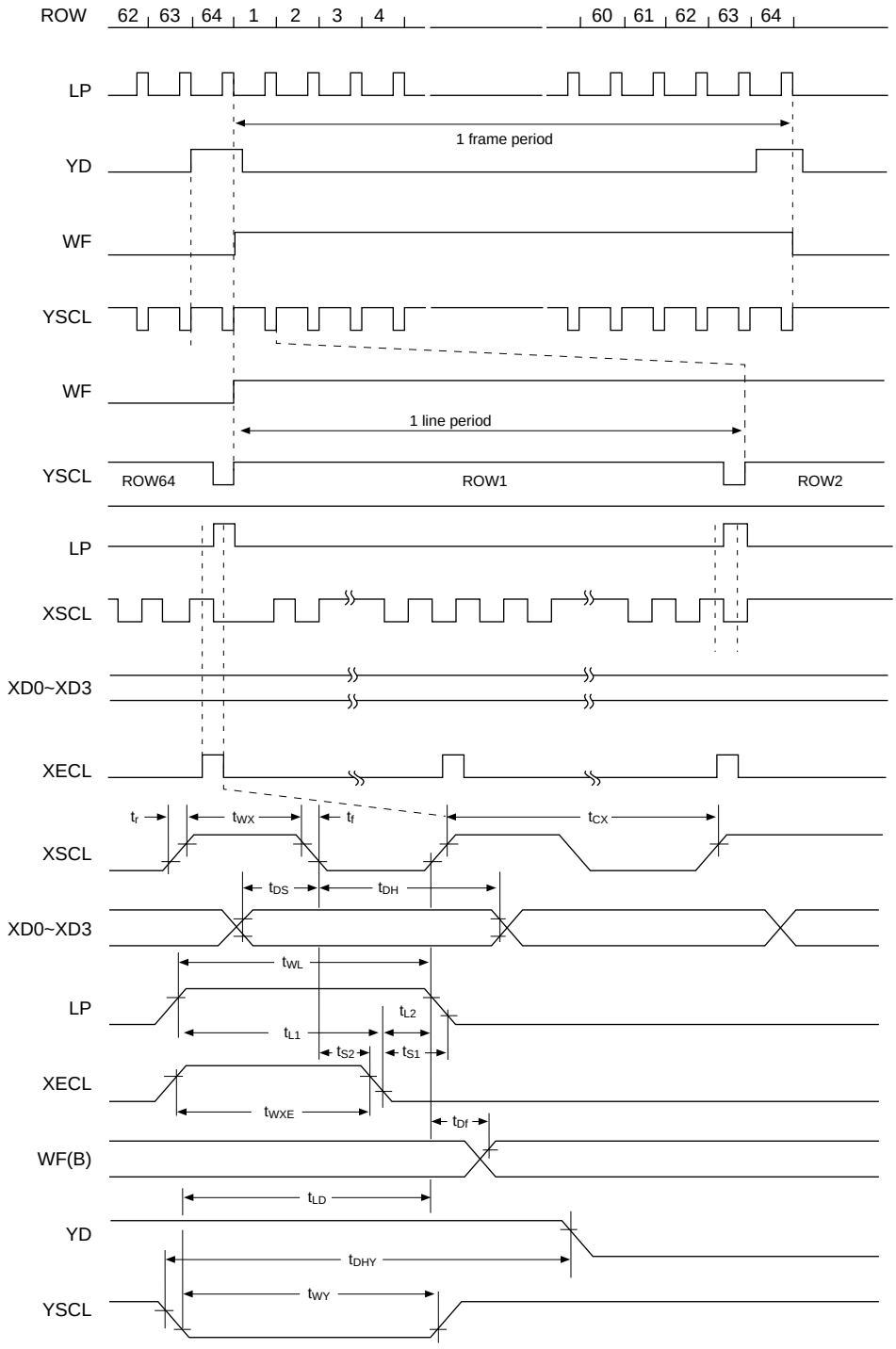


Figure 45. LCD output timing

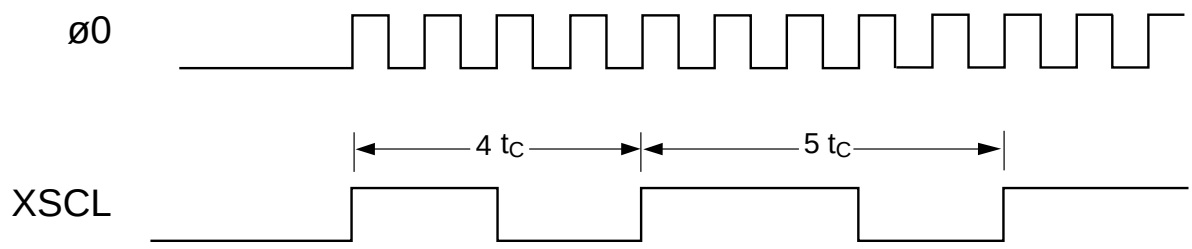
4.5.7.1 SED1330F

T_a = –20 to 75°C

Signal	Symbol	Parameter	Rating		Unit	Condition
			min	max		
	tr	$\overline{VCE}$ high level pulse width	—	35	ns	V_{DD} = 5.0V ±10% CL=150F
	tf	$\overline{VCE}$ low level pulse width	—	35	ns	
XSCL	tCX	Shift clock cycle time	4tc–70	—	ns	
	tWX	XSCL clock pulse width	2tC–80	—	ns	
XD0 to XD3	tDH	X-data hold time	2tC–100	—	ns	
	tDS	X-data setup time	2tC–100	—	ns	
LP	tLS	Latch data setup time	2tC–100	—	ns	
	tWL	LP signal pulse width	4tC–80	—	ns	
XECL	tL1	XECL setup time	3tC–100	—	ns	
	tL2	XECL data hold time	tC–30	—	ns	
	tS1	Enable setup time	tC–30	—	ns	
	tS1	Enable delay time	tC–30	—	ns	
	tWXE	XECL clock pulse width	3tC–80	—	ns	
WF	tDF	Time allowance of WF delay	—	100	ns	
YSCL	tLD	LP delay time against YSCL	4tC–100	—	ns	
	tWY	YSCL clock pulse width	4tC–80	—	ns	
YD	tDHY	Y-data hold time	6tC–100	—	ns	

Notes:

1. The E-1330 reads display memory data from the address of the top left corner of the display screen, then scans horizontally until it reaches the address for the bottom right corner of the display screen. Therefore, each line of X-driver data is sent starting from the left side of the display line.
2. The E-1330 uses nine cycles of ø0 as the basic cycle (t_c). The XSCL waveform is shown in the following figure.



4.5.7.2 SED1335F

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
	t_r	Rise time	—	30	—	40	ns	CL = 100 pF
	t_f	Fall time	—	30	—	40	ns	
XSCL	t_{CX}	Shift clock cycle time	4t_C	—	4t_C	—	ns	
	t_{WX}	XSCL clock pulsewidth	2t_C – 60	—	2t_C – 60	—	ns	
XD0 to XD3	t_{DH}	X data hold time	2t_C – 50	—	2t_C – 50	—	ns	
	t_{DS}	X data setup time	2t_C – 100	—	2t_C – 105	—	ns	
LP	t_{LS}	Latch data setup time	2t_C – 50	—	2t_C – 50	—	ns	
	t_{WL}	LP pulsewidth	4t_C – 80	—	4t_C – 120	—	ns	
	t_{LD}	LP delay time from XSCL	0	—	0	—	ns	
WF	t_{DF}	Permitted WF delay	—	50	—	50	ns	
YD	t_{DHY}	Y data hold time	2t_C – 20	—	2t_C – 20	—	ns	

4.5.7.3 SED1336F

T_a = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 3.0 to 4.5V		Unit	Condition
			min	max	min	max		
	t_r	Rise time	—	30	—	35	ns	CL = 100 pF
	t_f	Fall time	—	30	—	35	ns	
XSCL	t_{CX}	Shift clock cycle time	4t_C	—	4t_C	—	ns	
	t_{WX}	XSCL clock pulsewidth	2t_C – 60	—	2t_C – 60	—	ns	
XD0 to XD3	t_{DH}	X data hold time	2t_C – 50	—	2t_C – 50	—	ns	
	t_{DS}	X data setup time	2t_C – 100	—	2t_C – 100	—	ns	
LP	t_{LS}	Latch data setup time	2t_C – 50	—	2t_C – 50	—	ns	
	t_{WL}	LP pulsewidth	4t_C – 80	—	4t_C – 100	—	ns	
	t_{LD}	LP delay time from XSCL	0	—	0	—	ns	
WF	t_{DF}	Permitted WF delay	—	50	—	50	ns	
YD	t_{DHY}	Y data hold time	2t_C – 20	—	2t_C – 20	—	ns	

Note: The SED1335F/1336F reads display memory data from the address of the top left corner of the display screen, then scans horizontally until it reaches the address for the bottom right corner of the display screen. Therefore, each line of X-driver data is sent starting from the left side of the display line.

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5.0
Display Control Functions

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5.0 Display Control Functions

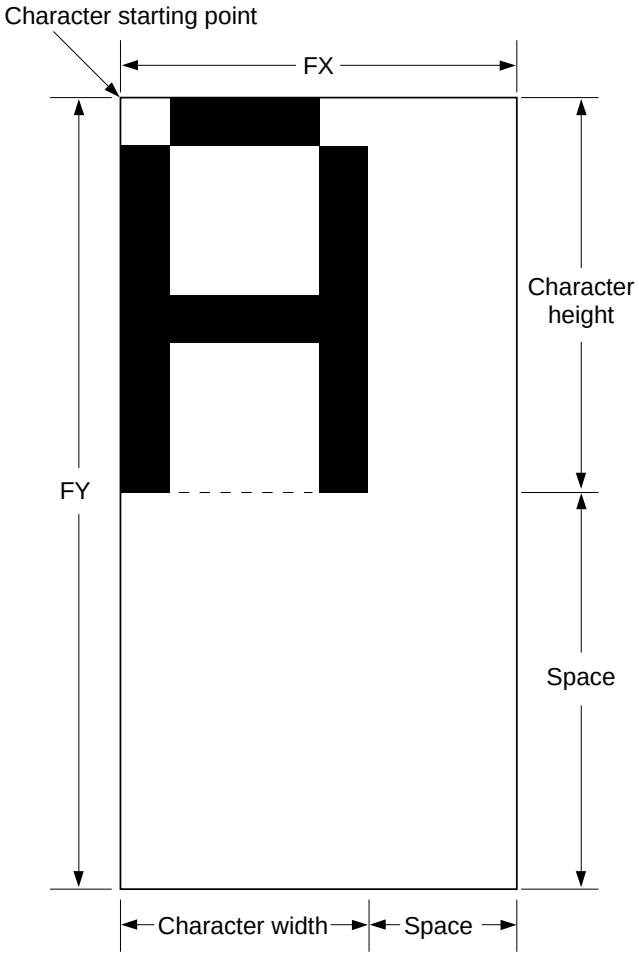
5.1 Character Configuration

The origin of each character bitmap is in the top left corner as shown in Figure 38. Adjacent bits in each byte are horizontally adjacent in the corresponding character image.

Although the size of the bitmap is fixed by the character generator, the actual displayed size of the character field can be varied in both dimensions.

If the area outside the character bitmap contains only zeros, the displayed character size can easily be increased by increasing FX and FY, as the zeros ensure that the extra space between displayed characters is blank.

The displayed character width can be set to any value up to 16 even if each horizontal row of the bitmap is two bytes wide.

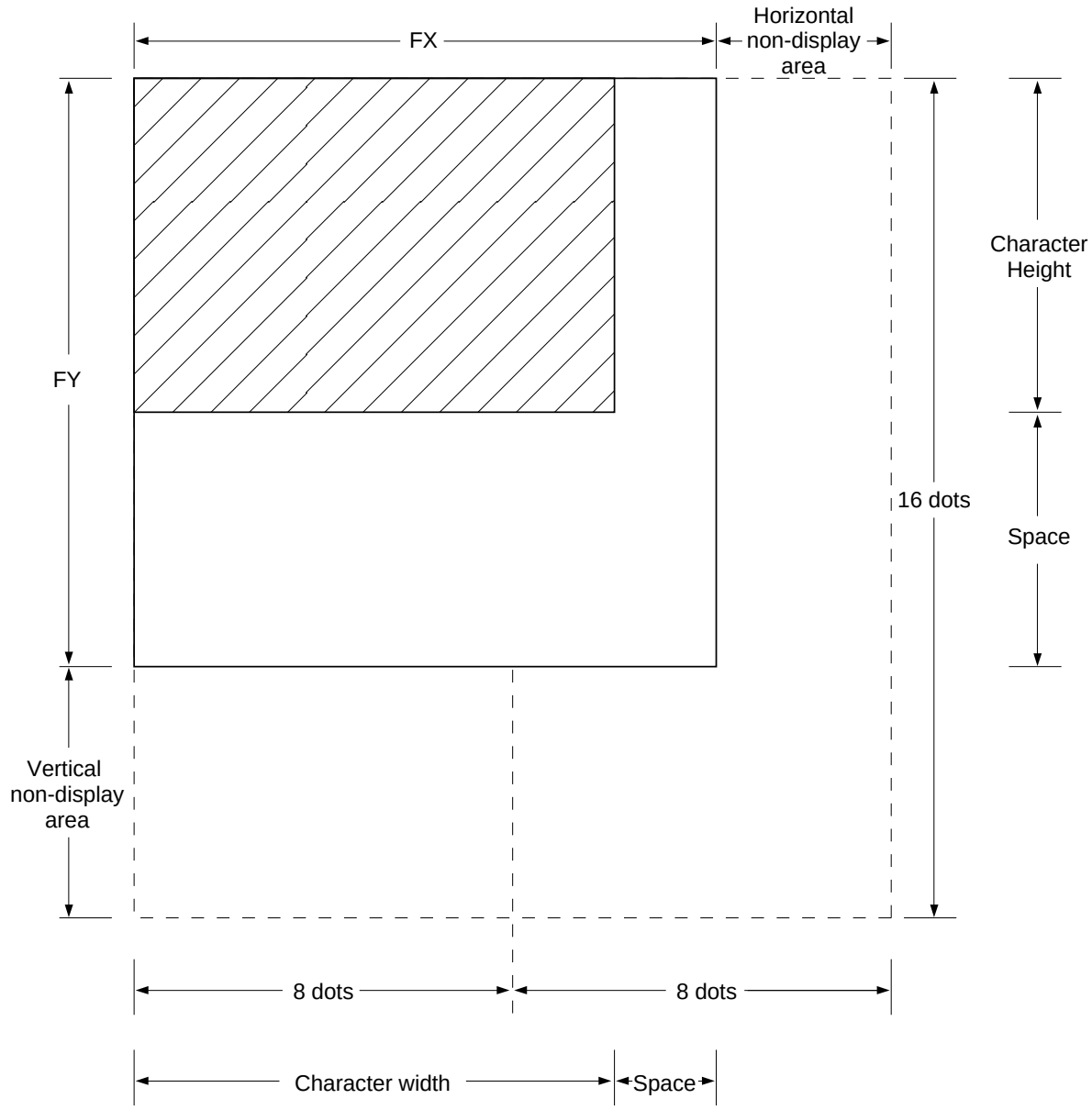


	D7			to			D0
R0	0	1	1	1	0	0	0	0
R1	1	0	0	0	1	0	0	0
R2	1	0	0	0	1	0	0	0
R3	1	0	0	0	1	0	0	0
R4	1	1	1	1	1	0	0	0
R5	1	0	0	0	1	0	0	0
R6	1	0	0	0	1	0	0	0
R7	0	0	0	0	0	0	0	0
R8	0	0	0	0	0	0	0	0
R9	0	0	0	0	0	0	0	0
R10	0	0	0	0	0	0	0	0
R11	0	0	0	0	0	0	0	0
R12	0	0	0	0	0	0	0	0
R13	0	0	0	0	0	0	0	0
R14	0	0	0	0	0	0	0	0
R15	0	0	0	0	0	0	0	0

Space data

Space data

Figure 46. Example of character display ([FX] ≤ 8) and generator bitmap



Note: The SED1330F/1335F/1336F does not automatically insert spaces between characters. If the displayed character size is 8 pixels or less and the space between character origins is nine pixels or more, the bitmap must use two bytes per row, even though the character image requires only one.

Figure 47. Character width greater than one byte wide ([FX] = 9)

5.2 Screen Configuration

5.2.1 Screen Configuration

The basic screen configuration of the SED1330F/1335F/1336F is as a single text screen or as overlapping text and graphics screens. The graphics screen uses eight times as much display memory as the text screen.

Figure 40 shows the relationship between the virtual screens and the physical screen.

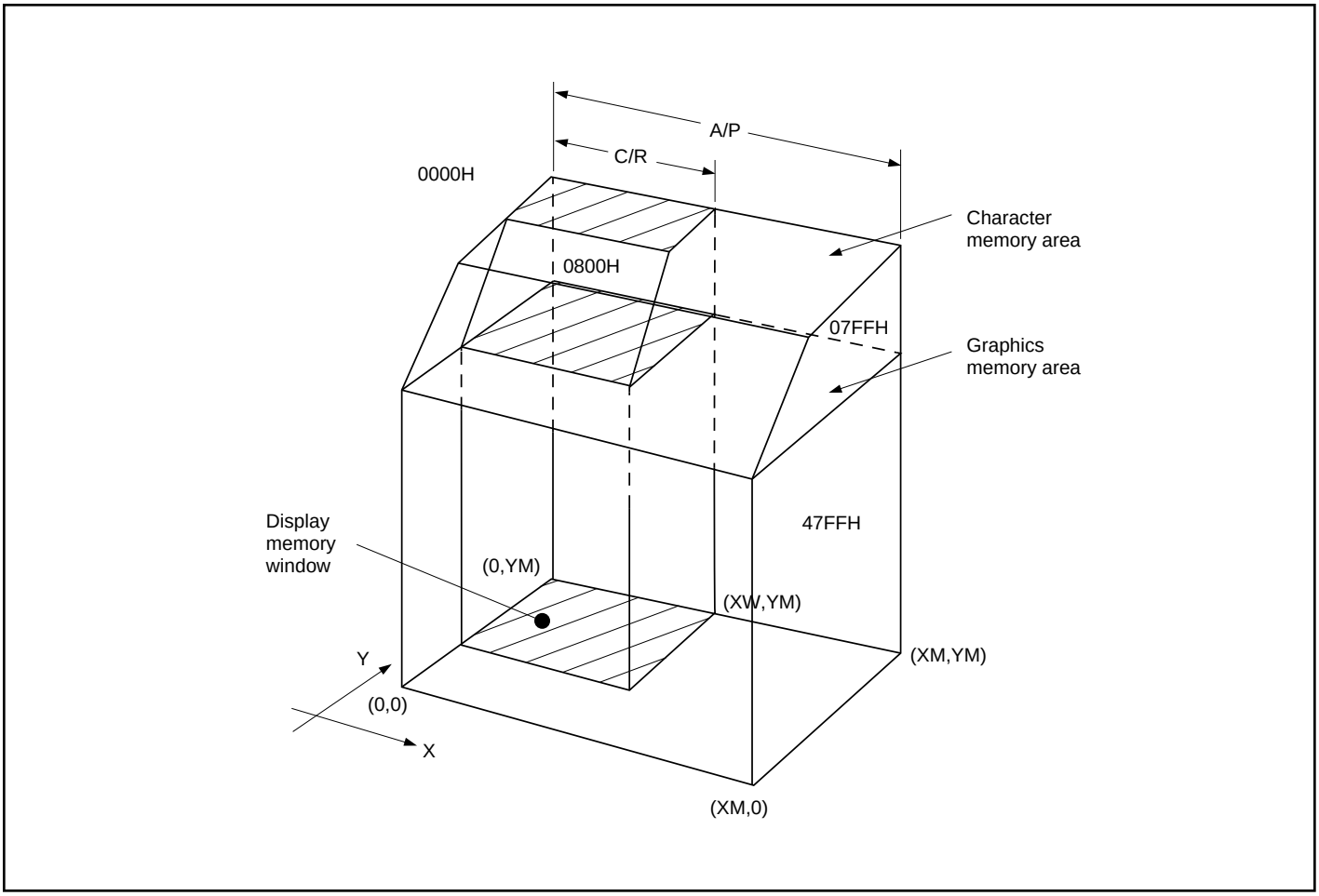


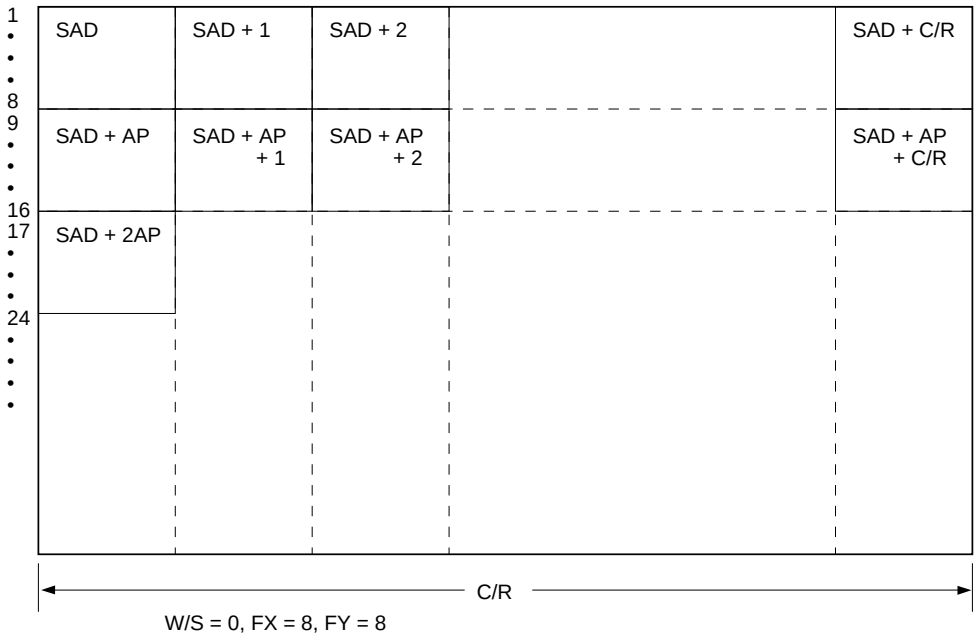
Figure 48. Virtual and physical screen relationship

5.2.2 Display Address Scanning

The SED1330F/1335F/1336F scans the display memory in the same way as a raster scan CRT screen. Each row is scanned from left to right until the address range equals C/R. Rows are scanned from top to bottom.

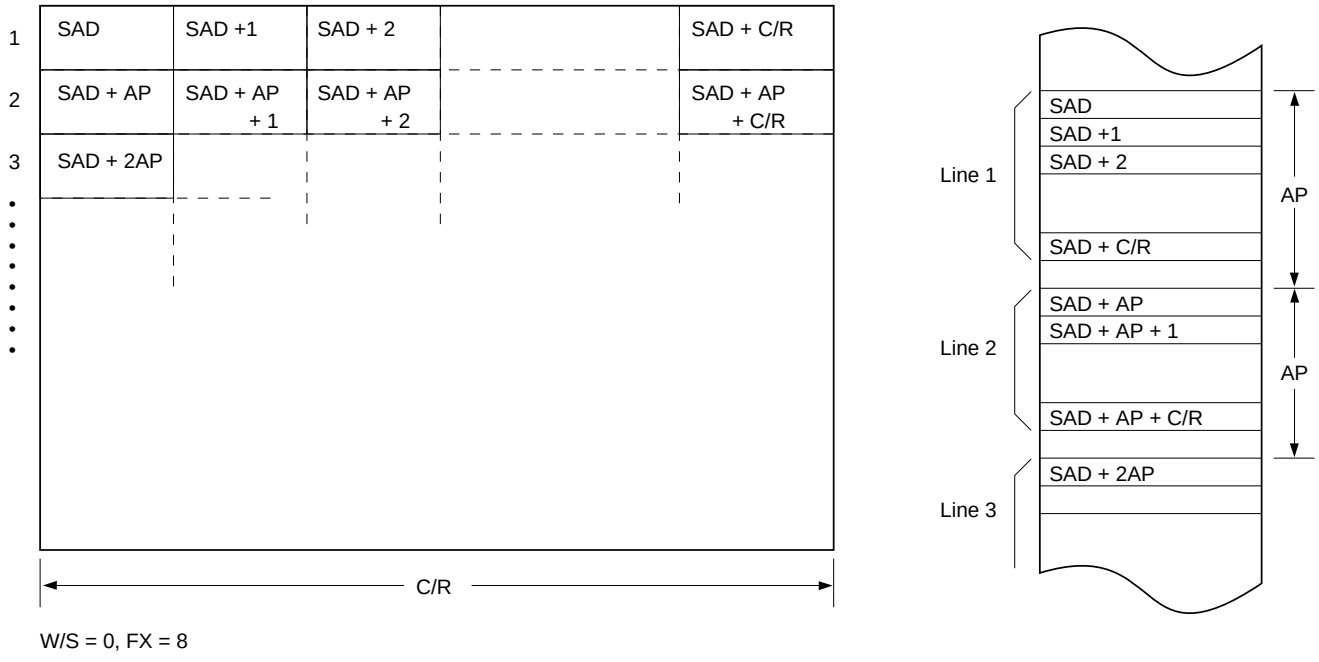
In graphics mode, at the start of each line, the address counter is set to the address at the start of the previous line plus the address pitch, AP.

In text mode, the address counter is set to the same start address, and the same character data is read, for each row in the character bitmap. However, a new row of the character generator output is used each time. Once all the rows in the character bitmap have been displayed, the address counter is set to the start address plus AP and the next line of text is displayed.



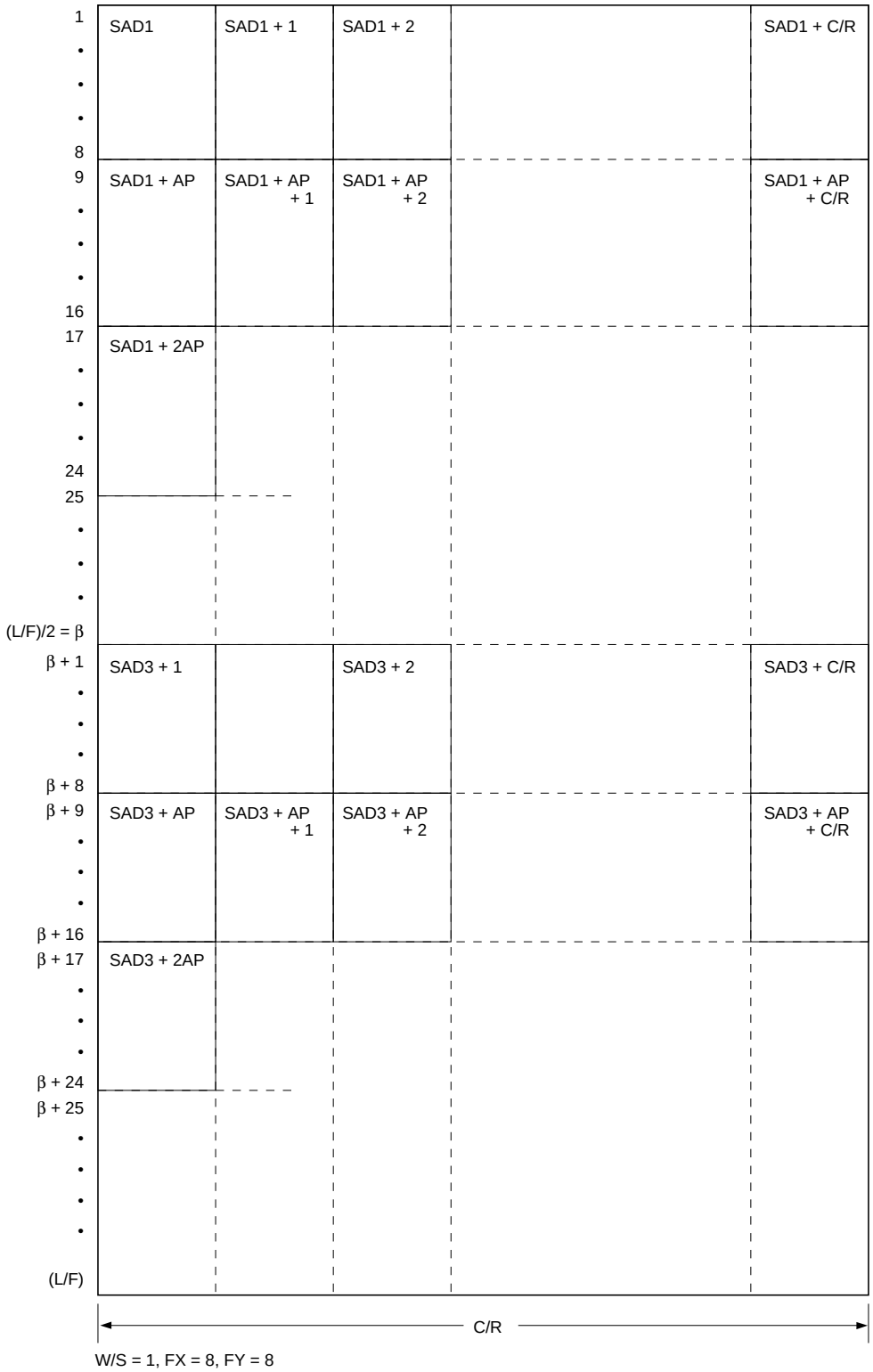
Note: One byte of display memory corresponds to one character.

Figure 49. Character position parameters



Note: One bit of display memory corresponds to one pixel.

Figure 50. Character parameters vs. memory



Note: In two-panel drive, the SED1330F/1335F/1336F reads line 1 and line β + 1 as one cycle. The upper and lower panels are thus read alternately, one line at a time.

Figure 51. Two-panel display address indexing

5.2.3 Display Scan Timing

Figure 44 shows the basic timing of the SED1330F/1335F/1336F. One display memory read cycle takes nine periods of the system clock, $\phi 0$ (f_{OSC}). This cycle repeats (C/R + 1) times per display line.

When reading, the display memory pauses at the end of each line for (TC/R – C/R) display memory read cycles, though the LCD drive signals are still generated. TC/R may be set to any value within the constraints imposed by C/R, f_{OSC}, f_{FR}, and the size of the LCD panel, and it may be used to fine tune the frame frequency. The microprocessor may also use this pause to access the display memory data.

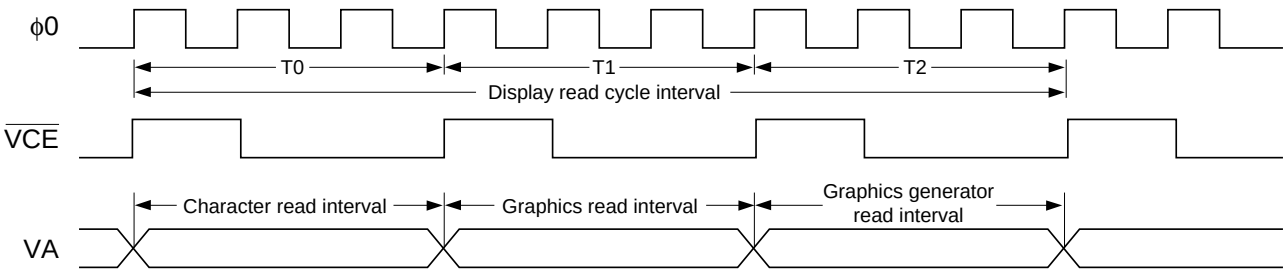
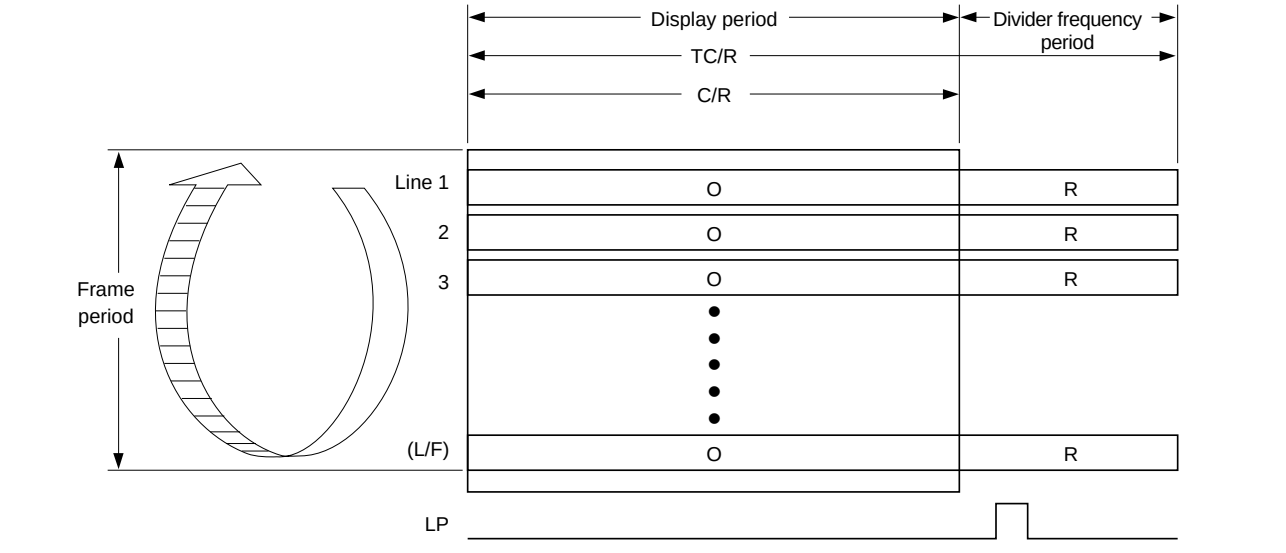


Figure 52. Display memory basic read cycle



Note: The divider adjustment interval (R) applies to both the upper and lower screens even if W/S = 1. In this case, LP is active only at the end of the lower screen's display interval.

Figure 53. Relationship between TC/R and C/R

5.3 Cursor Control

5.3.1 Cursor Register Function

The SED1330F/1335F/1336F cursor address register functions as both the displayed cursor position address register and the display memory access address register. When accessing display memory outside the actual screen memory, the address register must be saved before accessing the memory and restored after memory access is complete.

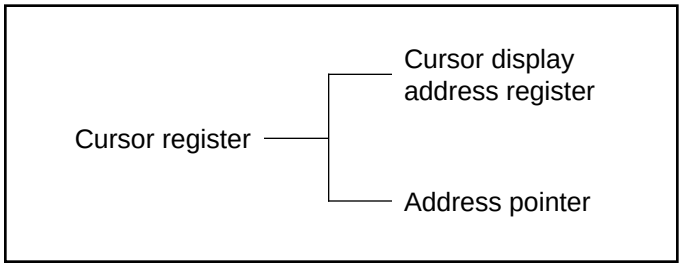


Figure 54. Cursor addressing

Note that the cursor may disappear from the display if the cursor address remains outside the displayed screen memory for more than a few hundred milliseconds.

5.3.2 Cursor Movement

On each memory access, the cursor address register changes by the amount previously specified with CSRDIR, automatically moving the cursor to the desired location.

5.3.3 Cursor Display Layers

Although the SED1330F/1335F/1336F can display up to three layers, the cursor is displayed in only one of these layers:

Two-layer configuration: First layer (L1)

Three-layer configuration: Third layer (L3)

The cursor will not be displayed if it is moved outside the memory for its layer. Layers may be swapped or the cursor layer moved within the display memory if it is necessary to display the cursor on a layer other than the present cursor layer.

Although the cursor is normally displayed for character data, the SED1330F/1335F/1336F may also display a dummy cursor for graphical characters. This is only possible if the graphics screen is displayed, the text screen is turned off and the microprocessor generates the cursor control address.

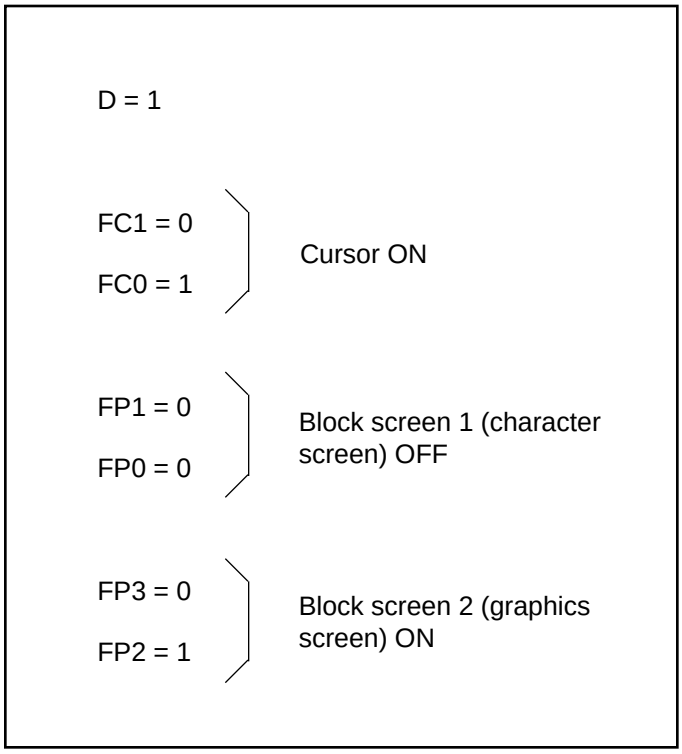


Figure 55. Cursor display layers

Consider the example of displaying Chinese characters on a graphics screen. To write the display data, the cursor address is set to the second screen block, but the cursor is not displayed. To display the cursor, the cursor address is set to an address within the blank text screen block.

Since the automatic cursor increment is in address units, not character units, the controlling microprocessor must set the cursor address register when moving the cursor over the graphical characters.

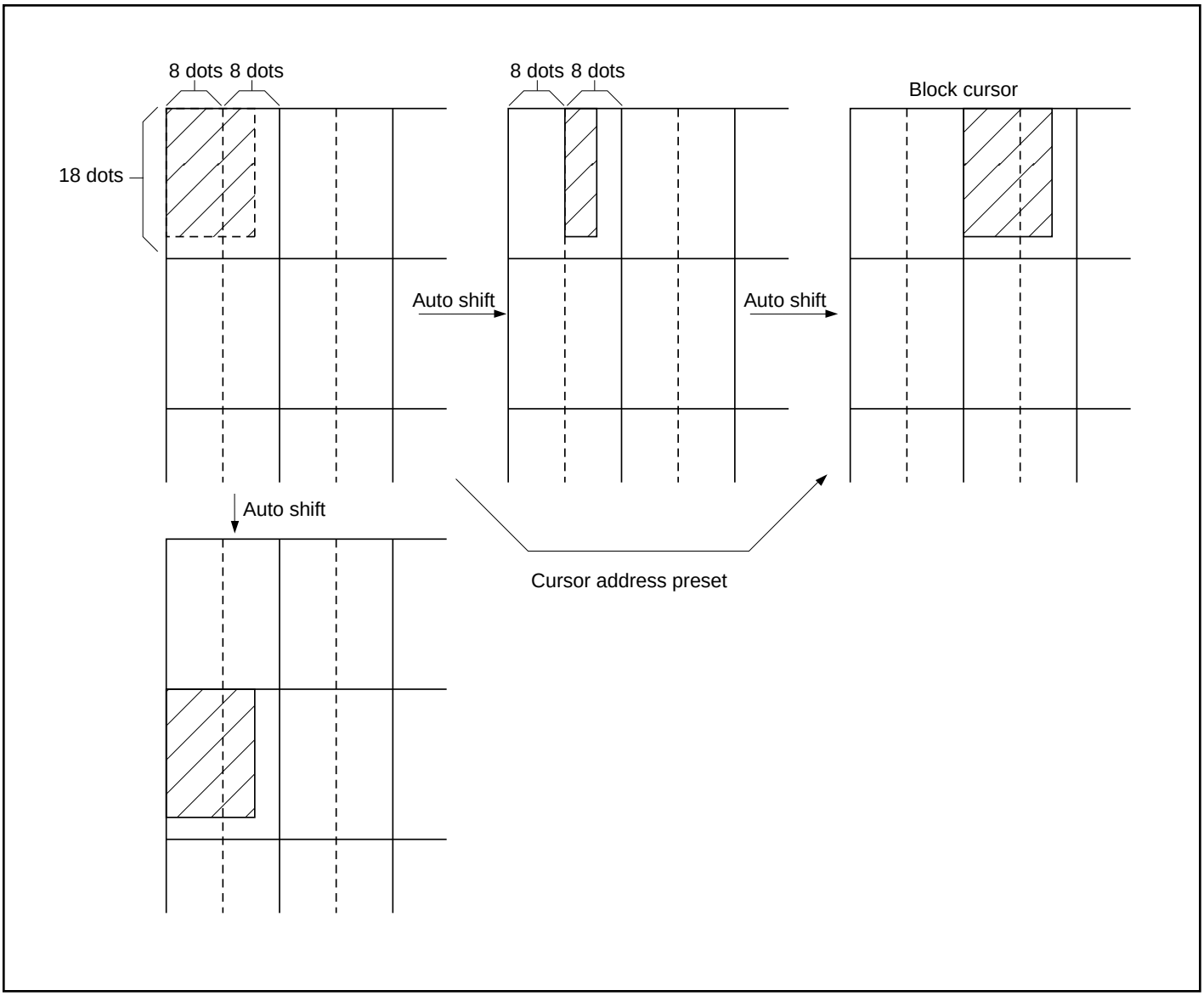


Figure 56. Cursor movement

If no text screen is displayed, only a bar cursor can be displayed at the cursor address.

If the first layer is a mixed text and graphics screen and the cursor shape is set to a block cursor, the SED1330F/1335F/1336F automatically decides which cursor shape to display. On the text screen it displays a block cursor, and on the graphics screen, a bar cursor.

5.4 Memory to Display Relationship

The SED1330F/1335F/1336F supports virtual screens that are larger than the physical size of the LCD panel address range, C/R. A layer of the SED1330F/1335F/1336F can be considered as a window in the larger virtual screen held in display memory. This window can be divided into two blocks, with each block able to display a different portion of the virtual screen.

This enables, for example, one block to dynamically scroll through a data area while the other acts as a status message display area. See Figure 49 and 50.

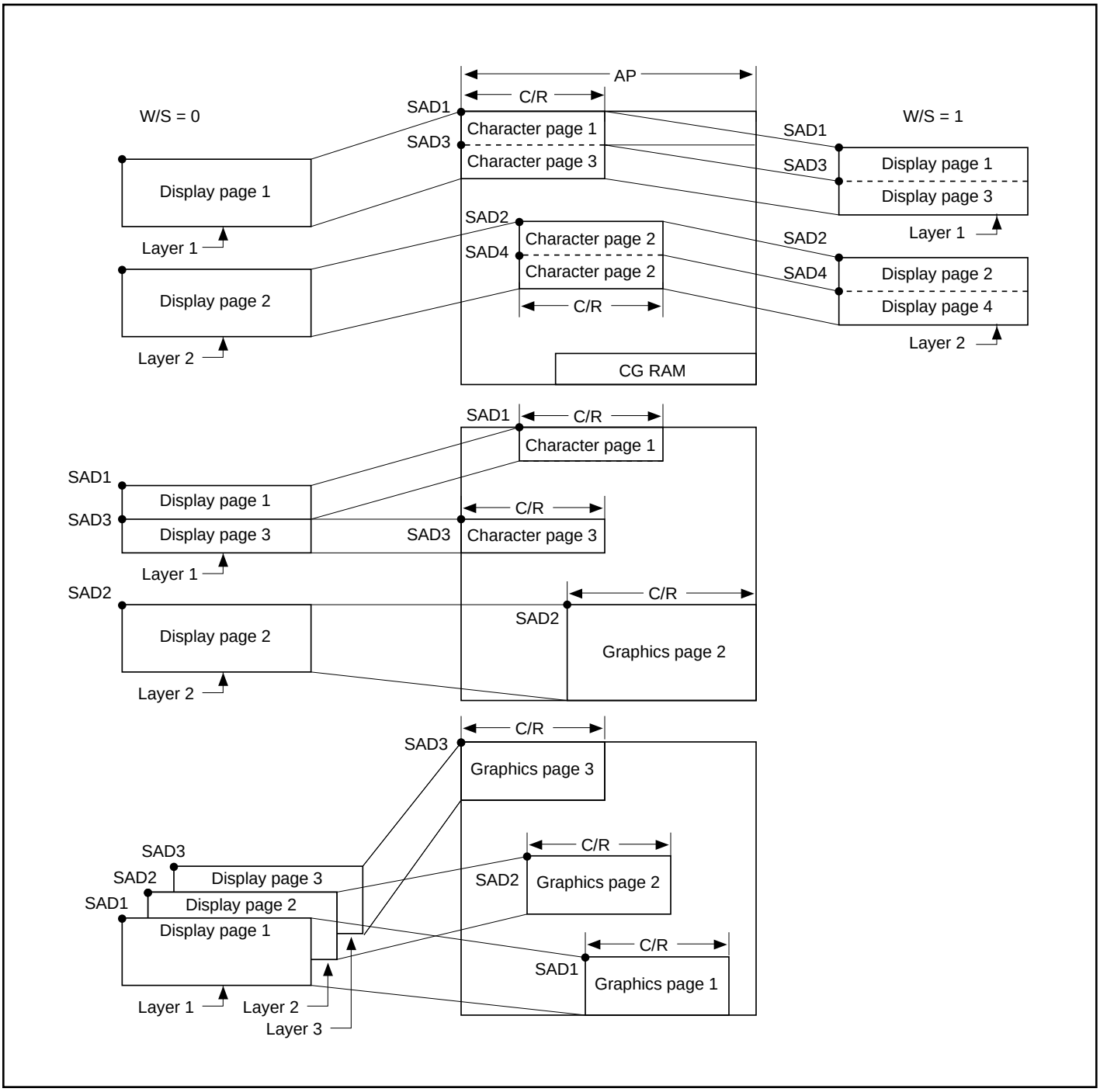


Figure 57. Display layers of memory

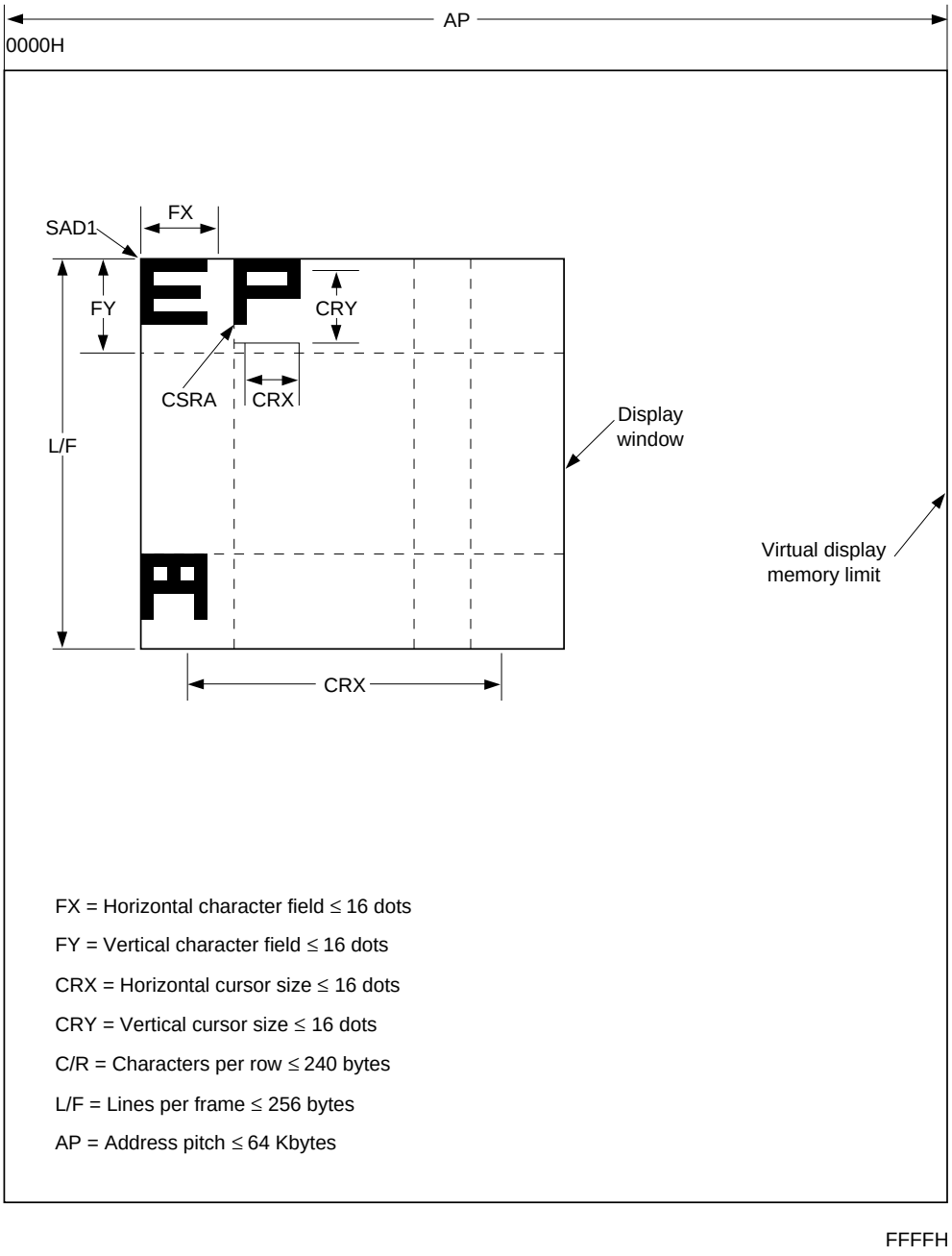


Figure 58. Display window and memory

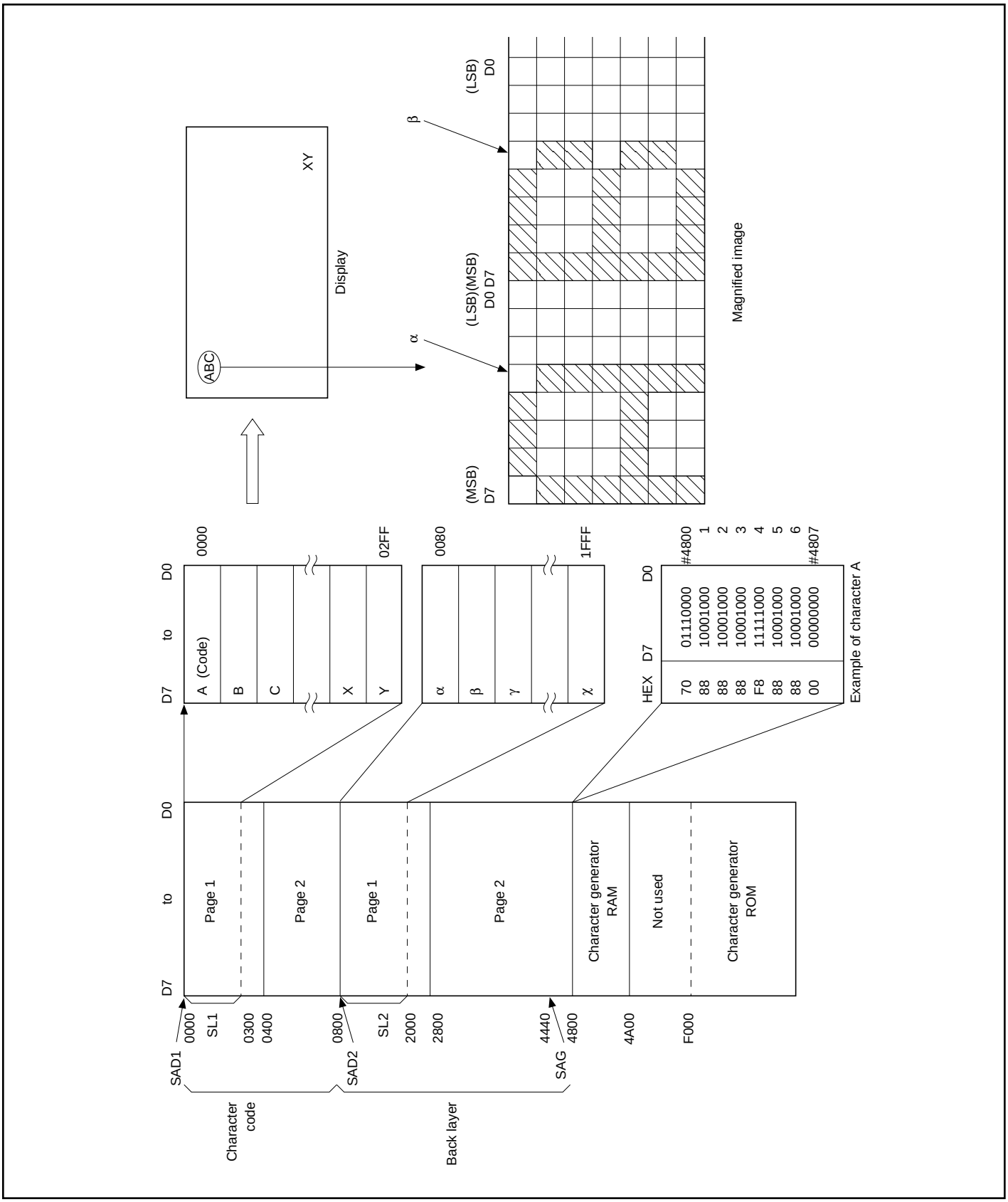


Figure 59. Memory map and magnified characters

5.5 Scrolling

The controlling microprocessor can set the SED1330F/1335F/1336F scrolling modes by overwriting the scroll address registers SAD1 to SAD4, and by directly setting the scrolling mode and scrolling rate.

5.5.1 On-page Scrolling

The normal method of scrolling within a page is to move the whole display up one line and erase the bottom line. Since the SED1330F/1335F/1336F does not automatically erase the bottom line, it must be erased with blanking data when changing the scroll address register.

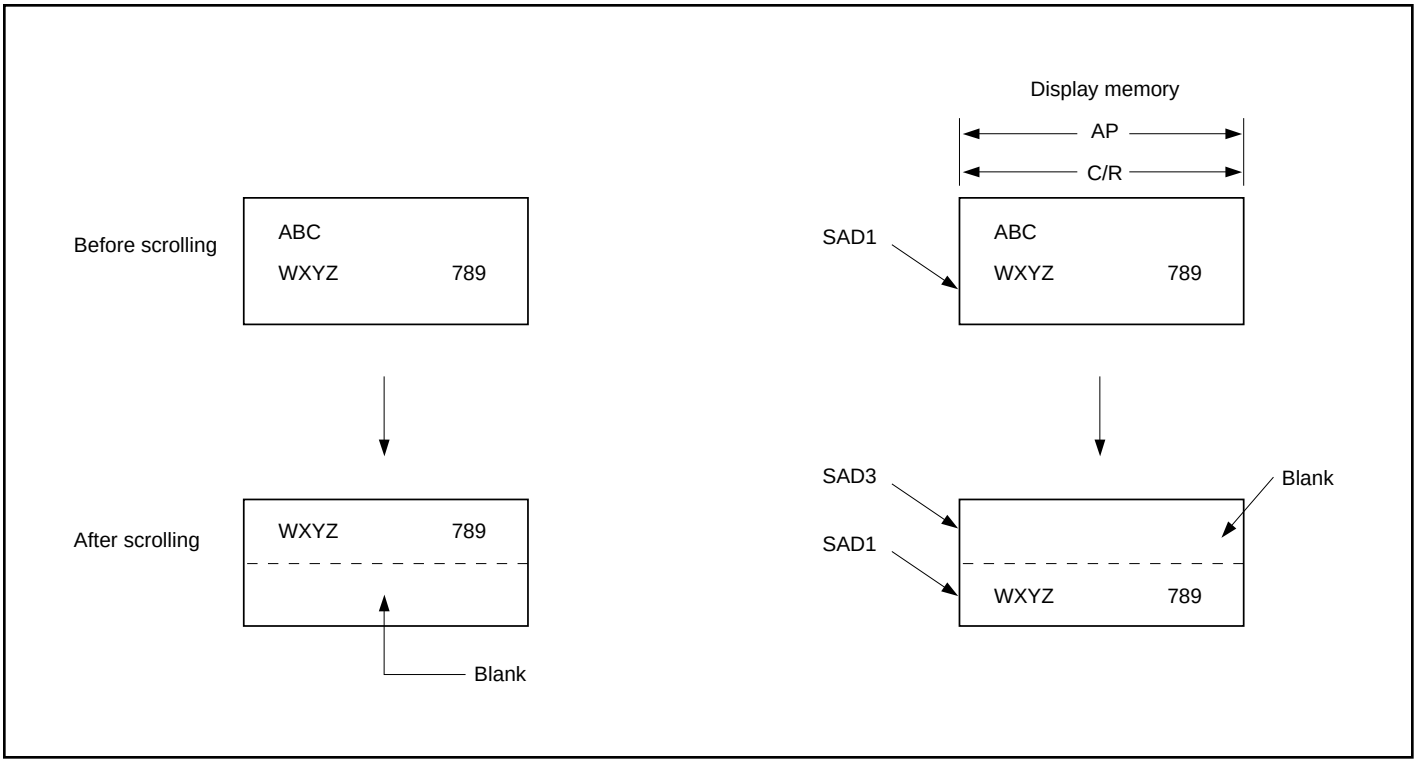


Figure 60. On-page scrolling

5.5.2 Inter-page Scrolling

Scrolling between pages and page switching can be performed only if the display memory capacity is greater than one screen.

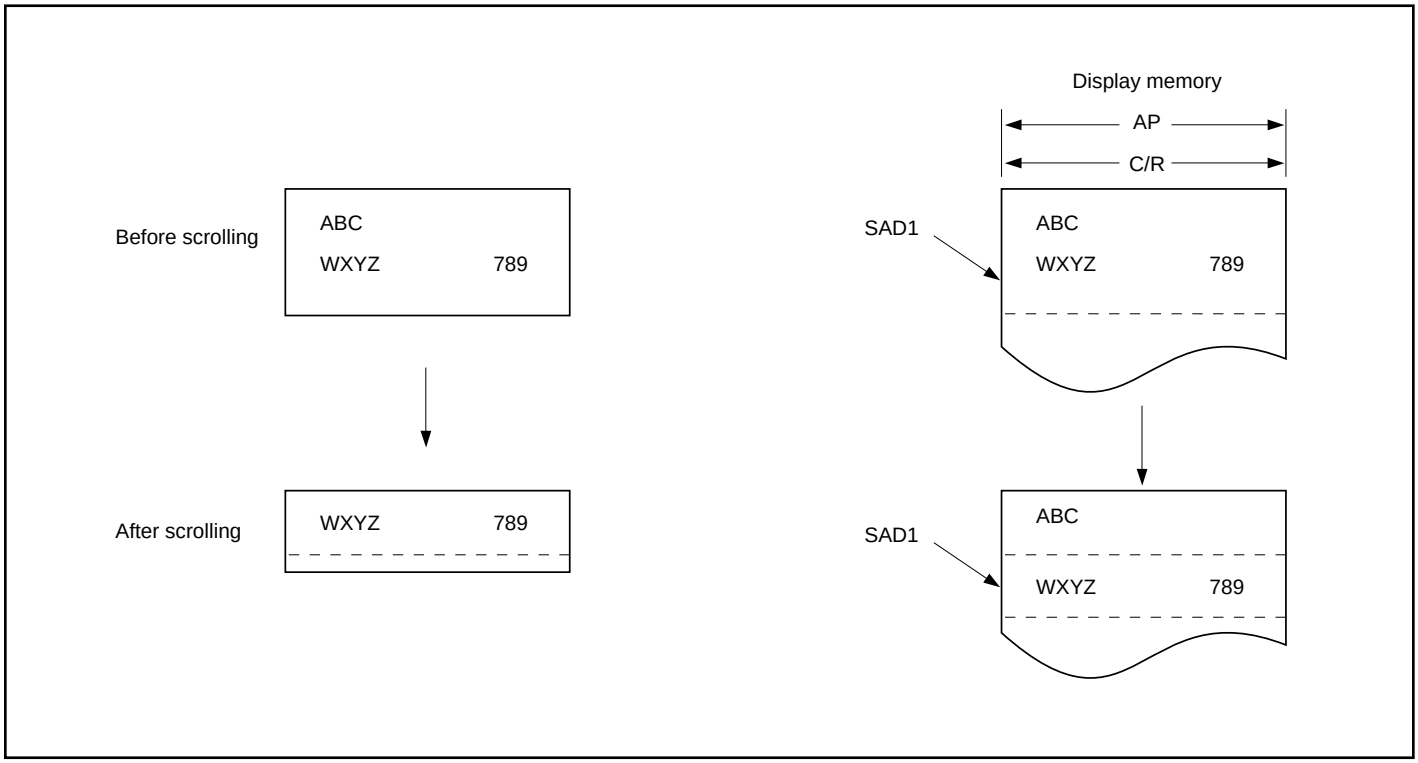


Figure 61. Inter-page scrolling

5.5.3 Horizontal Scrolling

The display can be scrolled horizontally in one-character units, regardless of the display memory capacity.

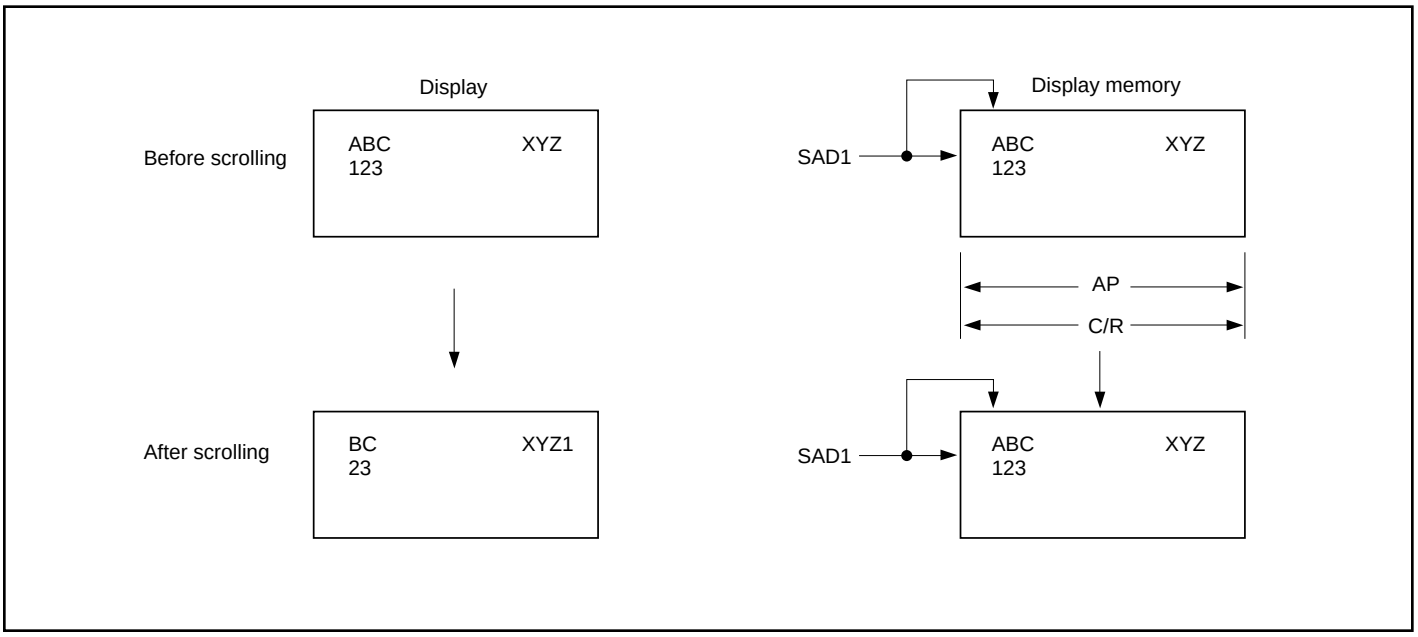


Figure 62. Horizontal wraparound scrolling

Refer to Section 9.4 for application notes.

5.5.4 Bidirectional Scrolling

Bidirectional scrolling can be performed only if the display memory is larger than the physical screen both horizontally and vertically. Although scrolling is normally done in single-character units, the HDOT SCR command can be used to scroll horizontally in pixel units. Single-pixel scrolling both horizontally and vertically can be performed by using the SCROLL and HDOT SCR commands. See Section 9.4

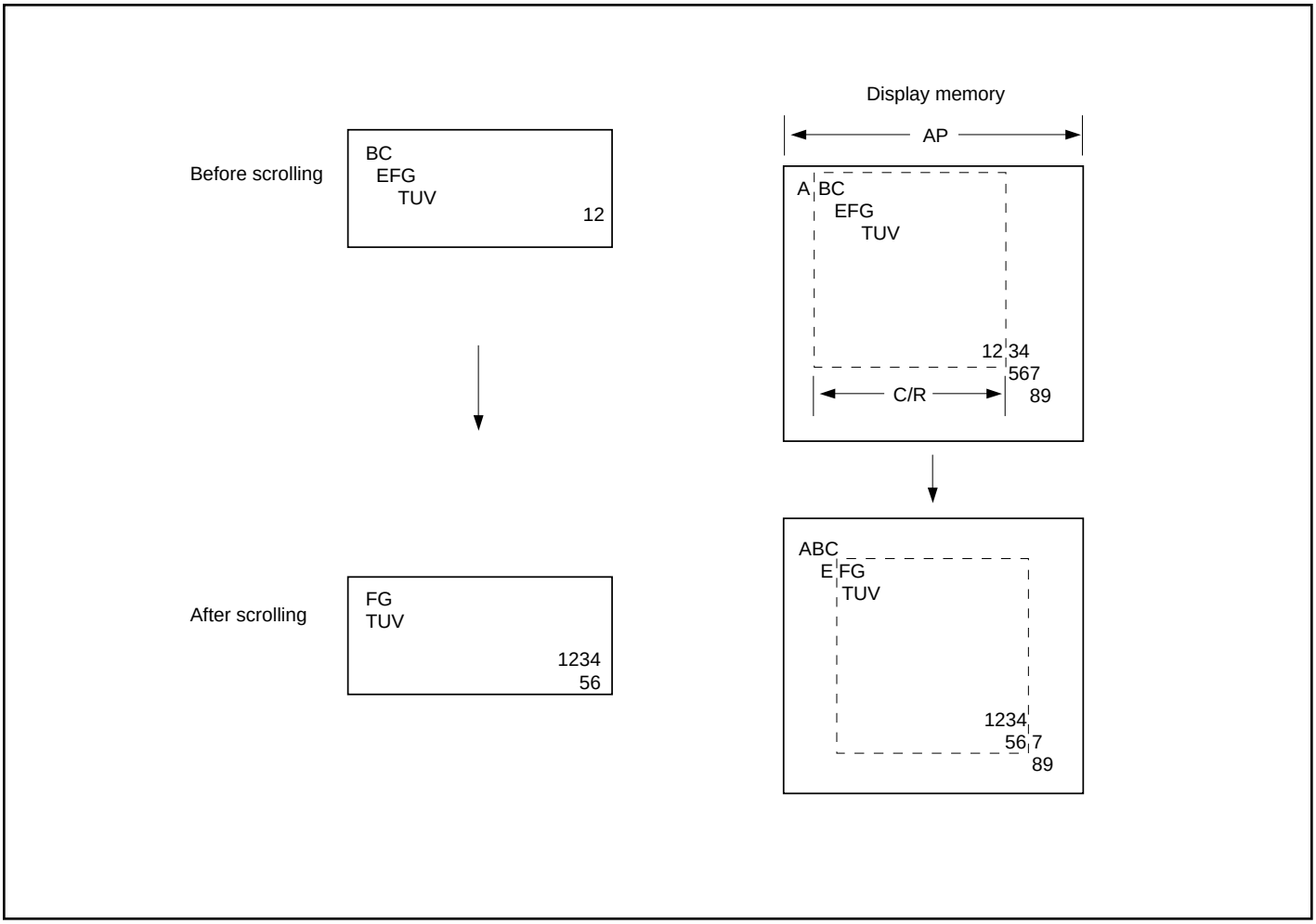


Figure 63. Bidirectional scrolling

5.5.5 Scroll Units

Table 21. Scroll units

Mode	Vertical	Horizontal
Text	Characters	Pixels or characters
Graphics	Pixels	Pixels

Note that in a divided screen, each block cannot be independently scrolled horizontally in pixel units.

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6.0
Character Generator

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6.0 Character Generator

6.1 CG Characteristics

6.1.1 Internal Character Generator

The internal character generator is recommended for minimum system configurations containing a SEDSED1330F/1335F/1336F, display RAM, LCD panel, single-chip microprocessor and power supply. Since the internal character generator uses a CMOS mask ROM, it is also recommended for low-power applications.

- 5 × 7-pixel font (See Section 10)
- 160 JIS standard characters
- Can be mixed with character generator RAM (maximum of 64 CG RAM characters)
- Can be automatically spaced out up to 8 × 16 pixels

6.1.2 External Character Generator ROM

The external CG ROM can be used when fonts other than those in the internal ROM are needed. Data is stored in the external ROM in the same format used in the internal ROM. (See Section 6.3.)

- Up to 8 × 8-pixel characters (M2 = 0) or 8 × 16-pixel characters (M2 = 1)
- Up to 256 characters (192 if used together with the internal ROM)
- Mapped into the display memory address space at F000H to F7FFH (M2 = 0) or F000H to FFFFH (M2 = 1)
- Characters can be up to 8 × 16-pixels; however, excess bits must be set to zero.

6.1.3 Character Generator RAM

The user can freely use the character generator RAM for storing graphics characters. The character generator RAM can be mapped by the microprocessor anywhere in display memory, allowing effective use of unused address space.

- Up to 8 × 8-pixel characters (M2 = 0) or 8 × 16 characters (M2 = 1)
- Up to 256 characters if mapped at F000H to FFFFH (64 if used together with character generator ROM)
- Can be mapped anywhere in display memory address space if used with the character generator ROM
- Mapped into the display memory address space at F000H to F7FFH if not used with the character generator ROM (more than 64 characters are in the CG RAM). Set SAG0 to F000H and M1 to zero when defining characters number 193 upwards.

6.2 CG Memory Allocation

Since the SED1335F/1336F uses 8-bit character codes, it can handle no more than 256 characters at a time. However, if a wider range of characters is required, character generator memory can be bank-switched using the CGRAM ADR command.

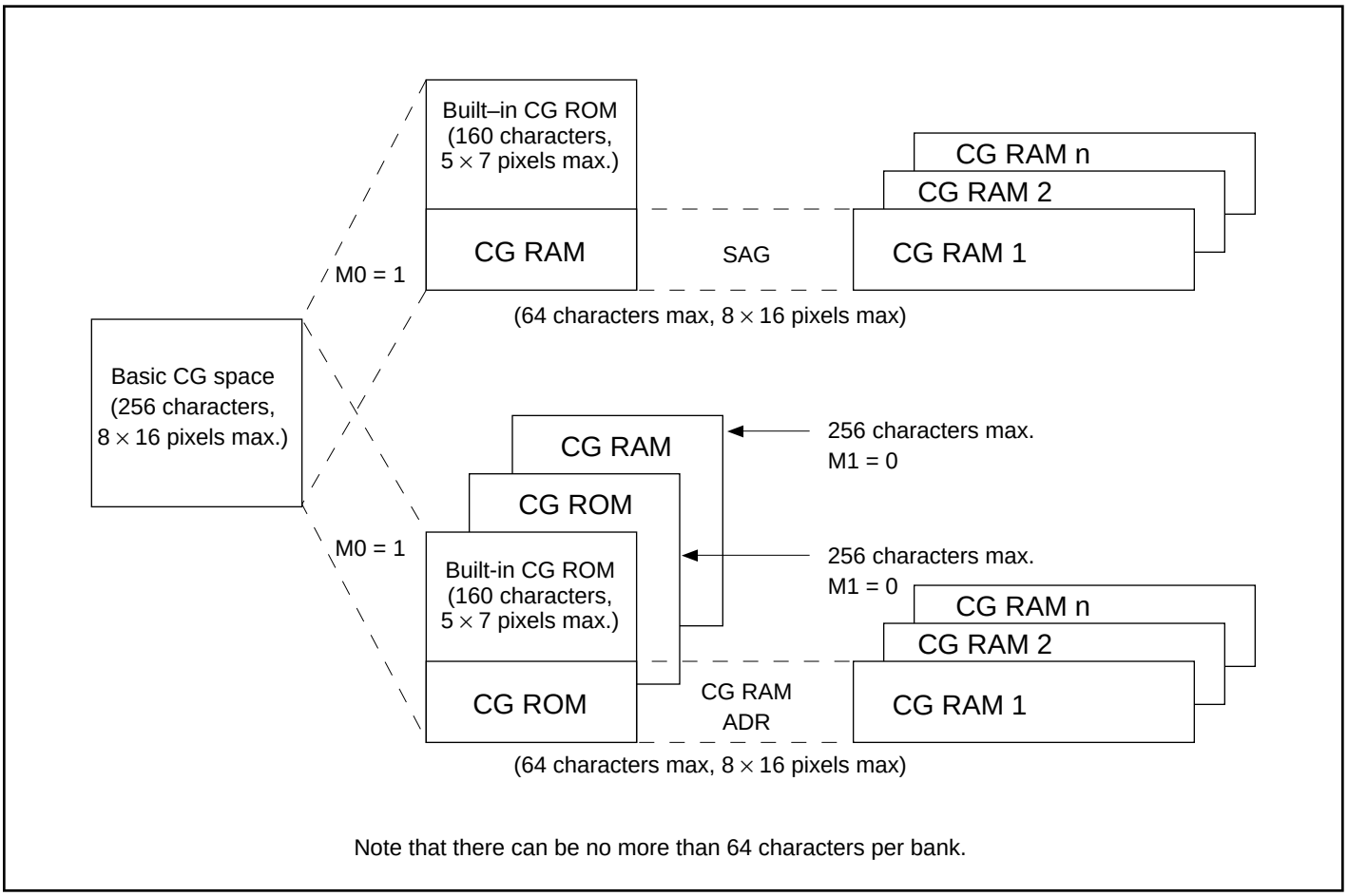


Figure 64. Internal and external character mapping

Table 22. Character mapping

Item		Parameter	Remarks
Internal/external character generator selection		M0	
Character field height	1 to 8 pixels	M2 = 0	
	9 to 16 pixels	M2 = 1	
	Greater than 16 pixels	Graphics mode (8 bits × 1 line)	
Internal CG ROM/RAM select		Automatic	Determined by the character code
External CG ROM/RAM select			
CG RAM bit 6 correction		M1	
CG RAM data storage address		Specified with CG RAM ADR command	Can be moved anywhere in the display memory address space
External CG ROM address	192 characters or less	Other than the area of Figure 58	
	More than 192 characters	Set SAG to F000H and overly SAG and the CG ROM table.	

6.3 Setting the Character Generator Address

The CG RAM addresses in the VRAM address space are not mapped directly from the address in the SAG register. The data to be displayed is at a CG RAM address calculated from SAG + character code + ROW select address. This mapping is shown in Tables 23 and 24.

Table 23. Character fonts, number of lines ≤ 8 (M2 = 0, M1 = 0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0
+ROW select address	0	0	0	0	0	0	0	0	0	0	0	0	0	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

Table 24. Character fonts, 9 ≤ number of lines ≤ 16 (M2 = 1, M1 = 0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
+ROW select address	0	0	0	0	0	0	0	0	0	0	0	0	R3	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

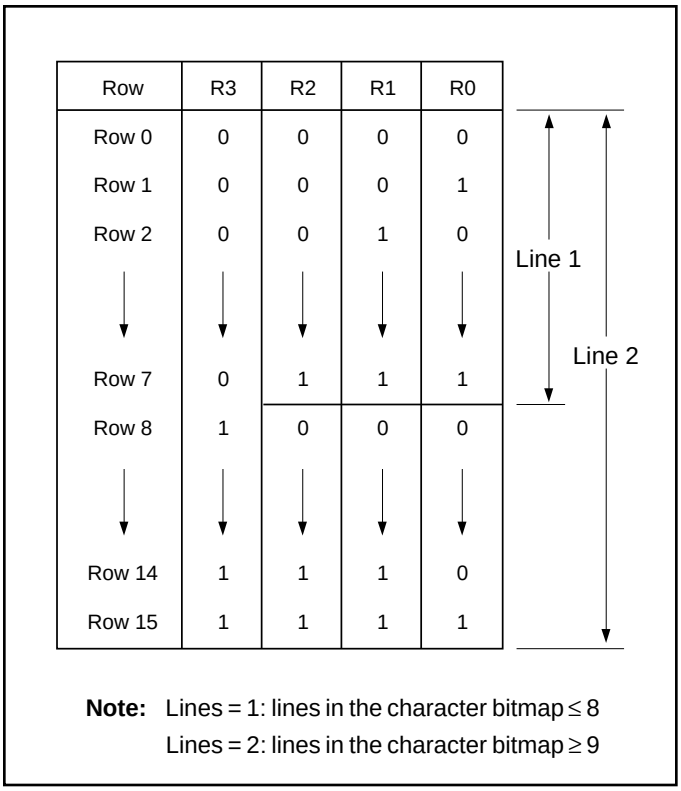


Figure 65. Row select address

6.3.1 M1 = 1

The SED1335F/1336F automatically converts all bits set in bit 6 of character code for CG RAM 2 to zero. Because of this, the CG RAM data areas become contiguous in display memory.

When writing data to CG RAM:

- Calculate the address as for M1 = 0.
- Change bit 6 of the character code from “1” to “0”.

6.3.2 CG RAM Addressing Example

- Define a pattern for the “A” in Figure 38.
- The CG RAM table start address is 4800H.
- The character code for the defined pattern is 80H (the first character code in the CG RAM area).

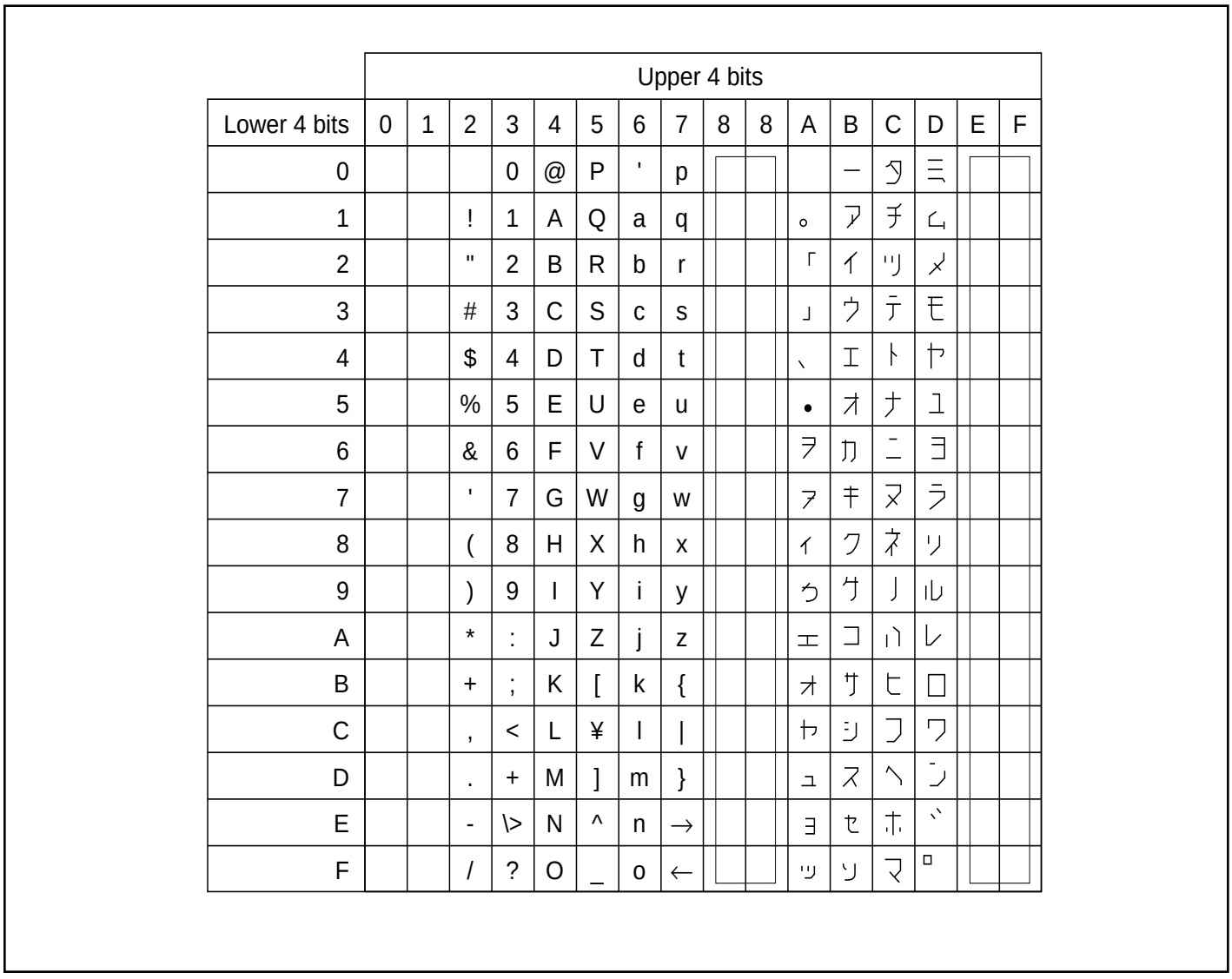
As the character code table in Figure 58 shows, codes 80H to 9FH and E0H to FFH are allocated to the CG RAM and can be used as desired. 80H is thus the first code for CG RAM. As characters cannot be used if only using graphics mode, there is no need to set the CG RAM data.

Table 25. Character data example

CGRAM ADR	5CH	Reverse the CG RAM address calculation to calculate SAG
P1	00H	
P2	40H	
CSRDIR	4CH	Set cursor shift direction to right
CSRW	46H	CG RAM start address is 4800H
P1	00H	
P2	48H	
MWRITE	42H	
P	70H	Write ROW 0 data
P2	88H	Write ROW 1 data
P3	88H	Write ROW 2 data
P4	88H	Write ROW 3 data
P5	F8H	Write ROW 4 data
P6	88H	Write ROW 5 data
P7	88H	Write ROW 6 data
P8	00H	Write ROW 7 data
P8	00H	Write ROW 8 data
↓	↓	↓
P16	00H	Write ROW 15 data

6.4 Character Codes

The following figure shows the character codes and the codes allocated to CG RAM. All codes can be used by the CG RAM if not using the internal ROM.



	Upper 4 bits															
Lower 4 bits	0	1	2	3	4	5	6	7	8	8	A	B	C	D	E	F
0				0	@	P	'	p				ー	タ	三		
1			!	1	A	Q	a	q			。	ア	チ	ム		
2			"	2	B	R	b	r			「	イ	ツ	メ		
3			#	3	C	S	c	s			」	ウ	テ	モ		
4			$	4	D	T	d	t			、	エ	ト	ヤ		
5			%	5	E	U	e	u			•	オ	ナ	ユ		
6			&	6	F	V	f	v			ヲ	カ	ニ	ヨ		
7			'	7	G	W	g	w			ァ	キ	ヌ	ラ		
8			(	8	H	X	h	x			ィ	ク	ネ	リ		
9			)	9	I	Y	i	y			ゥ	ケ	ノ	ル		
A			*	:	J	Z	j	z			ェ	コ	ハ	レ		
B			+	;	K	[	k	{			ォ	サ	ヒ	ロ		
C			,	<	L	¥	l	|			ャ	シ	フ	ワ		
D			.	+	M	]	m	}			ュ	ス	ヘ	ン		
E			-	\>	N	^	n	→			ョ	セ	ホ	゛		
F			/	?	O	_	o	←			ッ	ソ	マ	゜		

Figure 66. On-chip character codes

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7.0
TV Mode
(SED1336F only)

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7.0 TV Mode (SED1336F only)

When used with an external video mixer circuit, the SED1336F can show the same display on a television as on the LCD panel. In addition, the changeover from LCD-only to TV-and-LCD display is instantaneous with the changing of the T/L register using the System Set instruction.

The TV and LCD display register parameters which are determined by hardware constraints are shown in Table 26.

Table 26. Register parameters

System	TC/R (Hex)	C/R (Hex)	L/F (Hex)	Clock Cycles per Horizontal Line	Oscillator Frequency, fo (MHz)	T/L
NTSC	2A	1F	C7	388	6.1050	1
PAL	2A	1F	C7	388	6.0625	1
LCD	≥ 2A	1F	C7	≥ 388	6.0625 or 6.1050	0

7.1 Sync Generator Circuit Timing

The NTSC and PAL vertical sync signal waveforms are shown in Figure 59 and 60, respectively. The vertical sync timing parameters and VSD output states are shown in Table 27.

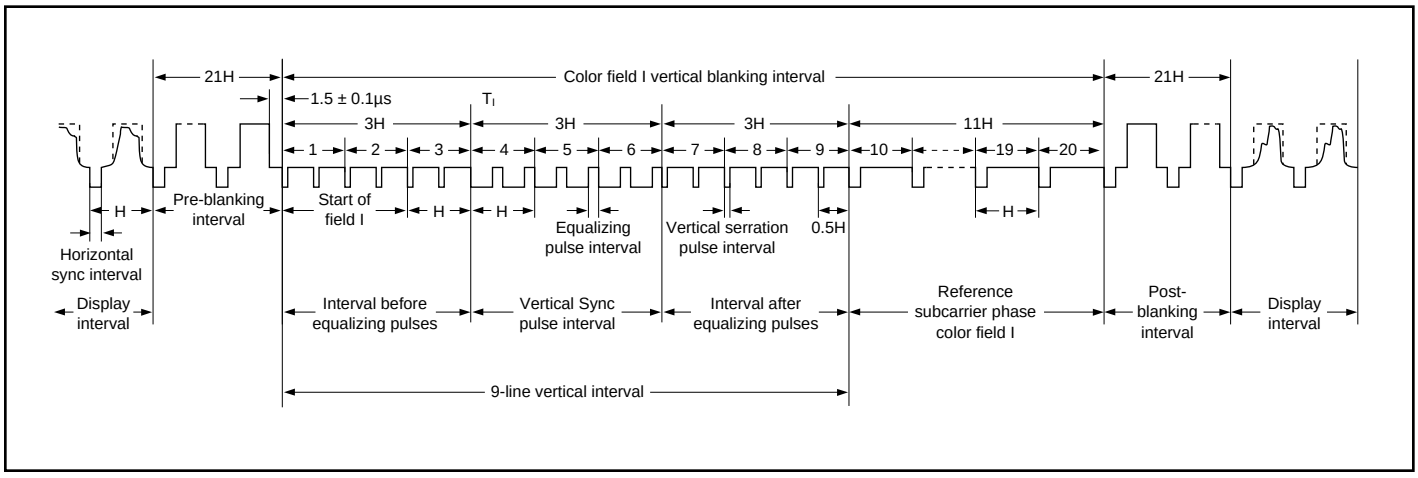

Figure 67. NTSC vertical sync waveform

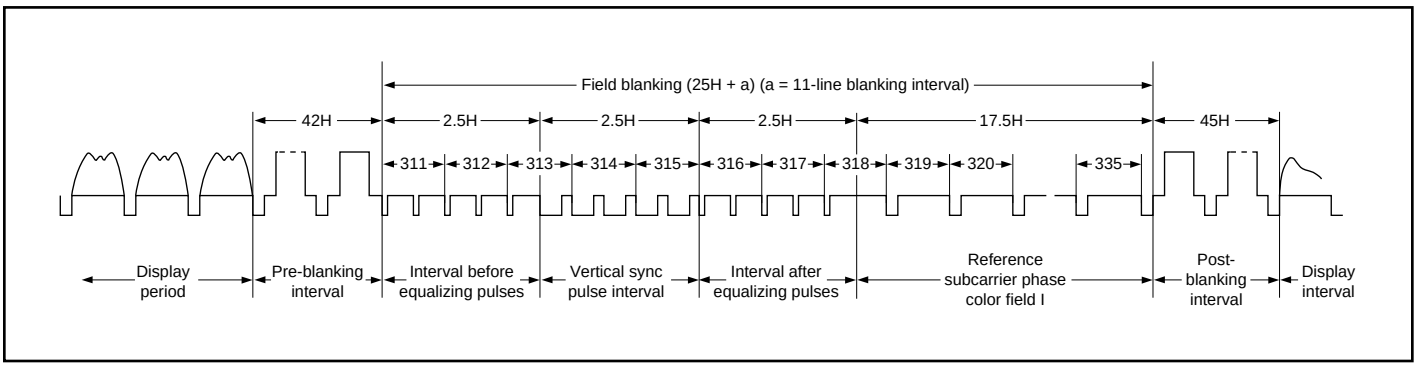

Figure 68. PAL vertical sync waveform

Table 27. Vertical sync timing characteristics

Parameter	Pre-blanking Interval	Interval before Equalizing Pulse	Vertical Sync Pulse Interval	Interval after Equalizing Pulse	Reference Subcarrier Phase Color Field I	Post-blanking Interval	Display Interval	Equalizing Pulse Interval	Vertical Serration Pulse Interval
NTSC system timing	21H	3H	3H	3H	11H	21H	200H	15CK	27CK
PAL system timing	42H	2.5H	2.5H	2.5H	17.5H	45H	200H	15CK	27CK
VSD output level	High impedance	LOW	LOW	LOW	LOW	High impedance	LOW or high impedance	—	—

Notes:

1. The NTSC system uses 262 lines per screen, and the PAL system, 312.
2. H = Horizontal line period
   CK = Oscillator period

The horizontal sync signal waveforms are shown in Figure 61, and the timing parameters and VSD output states, in Table 28. Note that SNC and VSD are both high-impedance when in LCD mode.

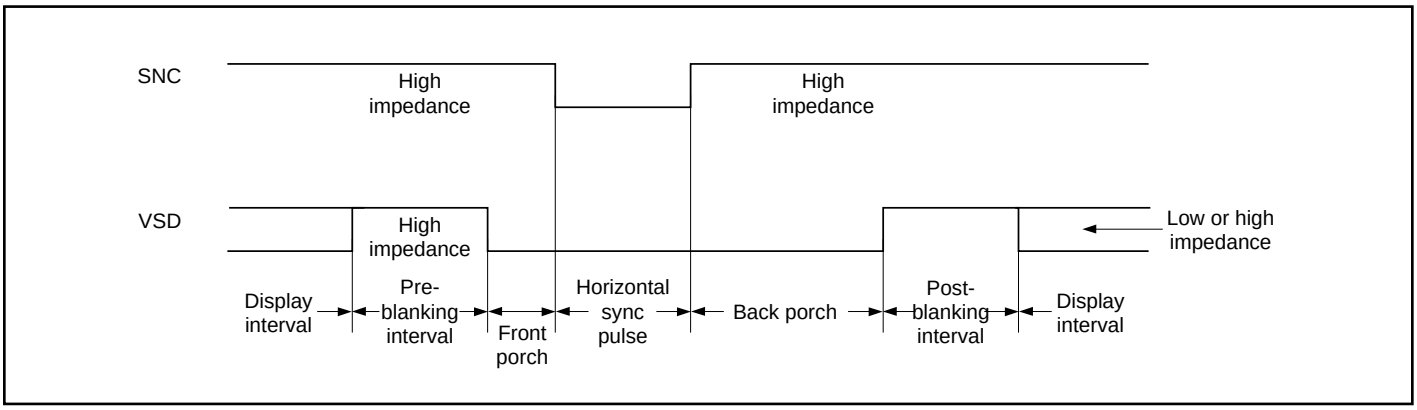

Figure 69. Horizontal sync waveforms

Table 28. Horizontal sync characteristics

Parameter	Pre-blanking Interval	Front Porch	Horizontal Sync Pulse	Back Porch	Post-blanking Interval	Display Interval
NTSC system timing	29CK	10CK	29CK	28CK	36CK	256CK
PAL system timing	29CK	10CK	29CK	34CK	30CK	256CK
VSD output level	High impedance	LOW	LOW	LOW	High impedance	LOW or High impedance

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8.0
Description of Circuit Blocks

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8.0 Description of Circuit Blocks

8.1 Microprocessor Interface

8.1.1 System Bus Interface

SEL1, SEL2 (SED1330F and SED1335F only), A0, $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ are used as control signals for the microprocessor data bus. A0 is normally connected to the lowest bit of the system address bus. SEL1 and SEL2 change the operation of the $\overline{RD}$ and $\overline{WR}$ pins to enable interfacing to either an 8080 or 6800 family bus, and should have either a pull-up or a pull-down resistor.

With microprocessors using an 8080 family interface, the SED1330F/1335F/1336F is normally mapped into the I/O address space.

8.1.1.1 8080 series

Table 29. 8080 series interface signals

A0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Status flag read
1	0	1	Display data and cursor address read
0	1	0	Display data and parameter write
1	1	0	Command write

8.1.1.2 6800 series

Table 30. 6800 series interface signals

A0	$\overline{RD}$	$\overline{WR}$	Function
0	1	1	Status flag read
1	1	1	Display data and cursor address read
0	0	1	Display data and parameter write
1	0	1	Command write

8.1.2 Microprocessor Synchronization

The SED1330F/1335F/1336F interface operates at full bus speed, completing the execution of each command within the cycle time, t_{CYC}. The controlling micro-processor's performance is thus not hampered by polling or handshaking when accessing the SED1330F/1335F/1336F.

Display flicker may occur if there is more than one consecutive access that cannot be ignored within a frame. The microprocessor can minimize this either by performing these accesses intermittently, or by continuously checking the status flag (D6) and waiting for it to become HIGH.

8.1.2.1 Display Status Indication Output (For SED1336 only)

When $\overline{CS}$, A0 and $\overline{RD}$ are LOW, D6 functions as the display status indication output. It is HIGH during the TV-mode vertical retrace period or the LCD-mode horizontal retrace period, and LOW, during the period the controller is writing to the display. By monitoring D6 and writing to the data memory only during retrace periods, the display can be updated without causing screen flicker.

8.1.2.2 Internal Register Access

The SYSTEM SET and SLEEP IN commands can be used to perform input/output to the SED1330F/1335F/1336F independently of the system clock frequency. These are the only commands that can be used while the SED1330F/1335F/1336F is in sleep mode.

8.1.2.3 Display Memory Access

The SED1330F/1335F/1336F supports a form of pipelined processing, in which the microprocessor

synchronizes its processing to the SED1330F/1335F/1336F's timing. When writing, the microprocessor first issues the MWRITE command. It then repeatedly writes display data to the SED1336F using the system bus timing. This ensures that the microprocessor is not slowed down even if the display memory access times are slower than the system bus access times. See Figure 70.

When reading, the microprocessor first issues the MREAD command, which causes the SED1330F/1335F/1336F to load the first read data into its output buffer. The microprocessor then reads data from the SED1330F/1335F/1336F using the system bus timing. With each read, the SED1330F/1335F/1336F reads the next data item from the display memory ready for the next read access. See Figure 71.

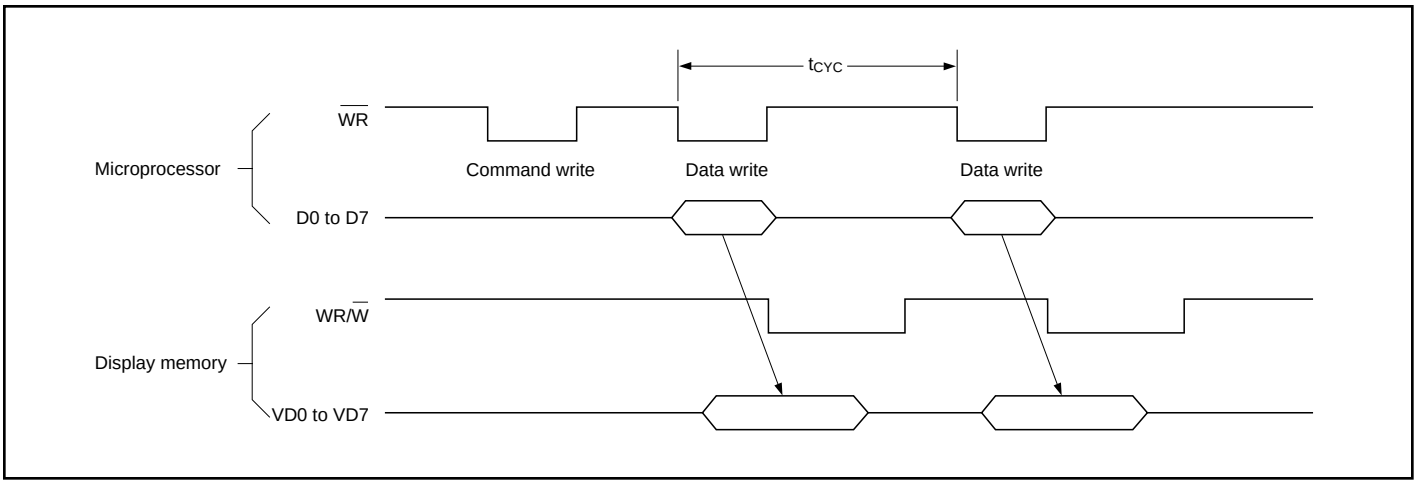


Figure 70. Display memory write cycle

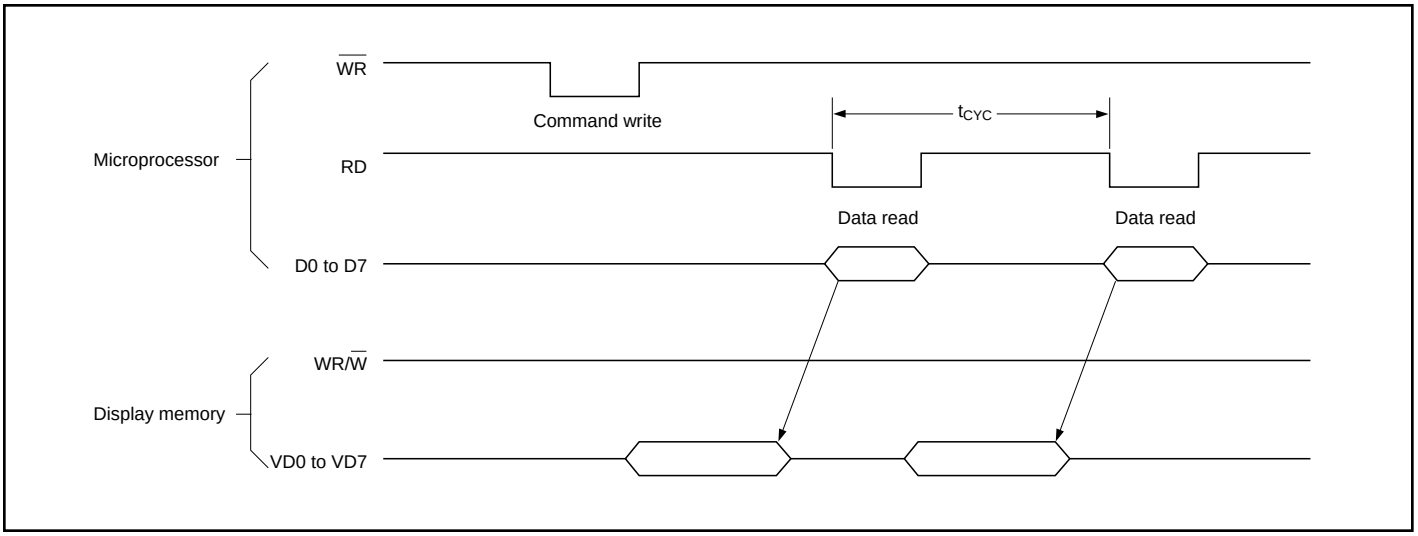
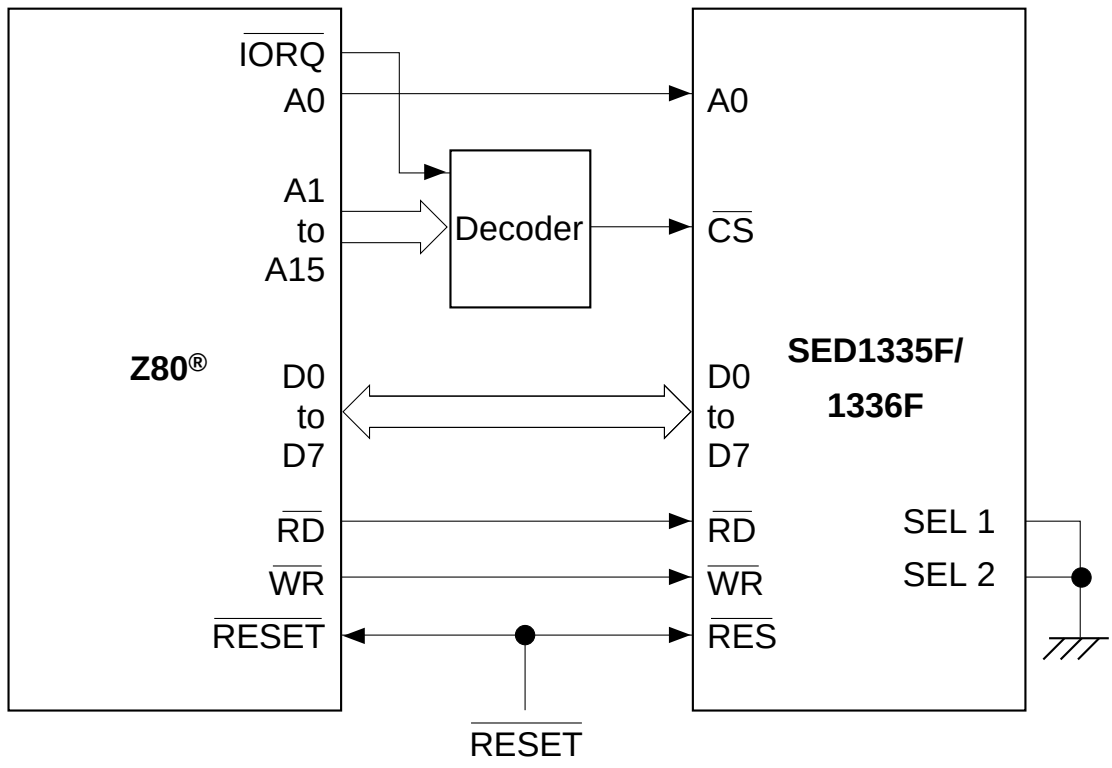


Figure 71. Display memory read cycle

Note: A possible problem with the display memory read cycle is that the system bus access time, t_{ACC}, does not depend on the display memory access time, t_{ACV}. The microprocessor may only make repeated reads if the read loop time exceeds the SED1330F/1335F/1336F cycle time, t_{CYC}. If it does not, NOP instructions may be inserted in the program loop. t_{ACC}, t_{ACV} and t_{CYC} limits are given in Section 4.3.

8.1.3 Interface Examples

8.1.3.1 Z80® to SED1330F/1335F/1336F Interface



Note: Z80® is a registered trademark of Zilog Corporation.

Figure 72. Z80® to SED1330F/1335F/1336F* interface

Note: *For SED1336F: SEL 2 is open..

8.1.3.2 6802 to SED1330F/1335F/1336F Interface

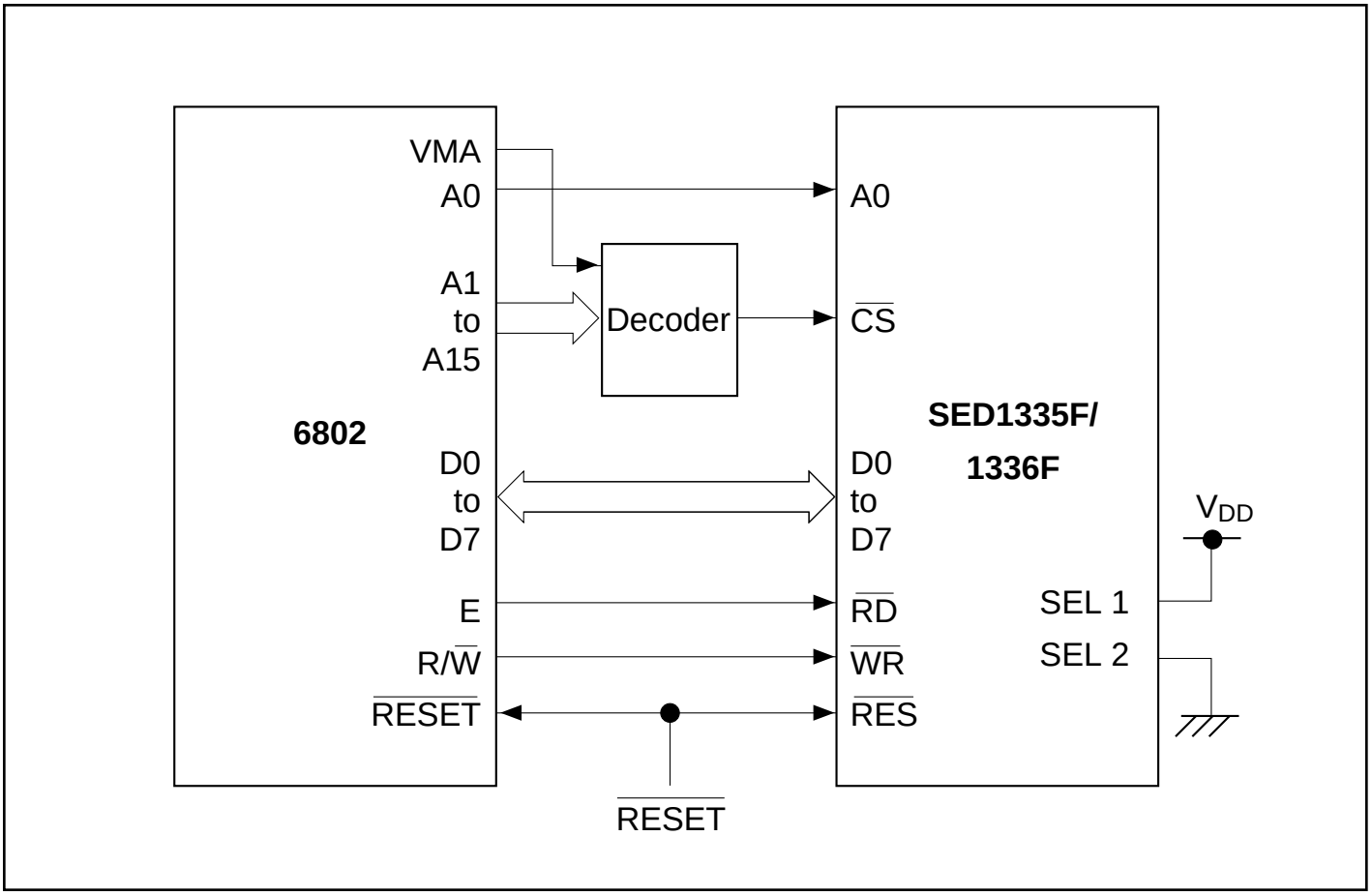


Figure 73. 6802 to SED1330F/1335F/1336F interface

Note: *For SED1336F: SEL 2 is open..

8.2 Display Memory Interface

8.2.1 Static RAM

The figure below shows the interface between an 8K × 8 static RAM and the SED1330F/1335F/1336F. Note that bus buffers are required if the bus is heavily loaded.

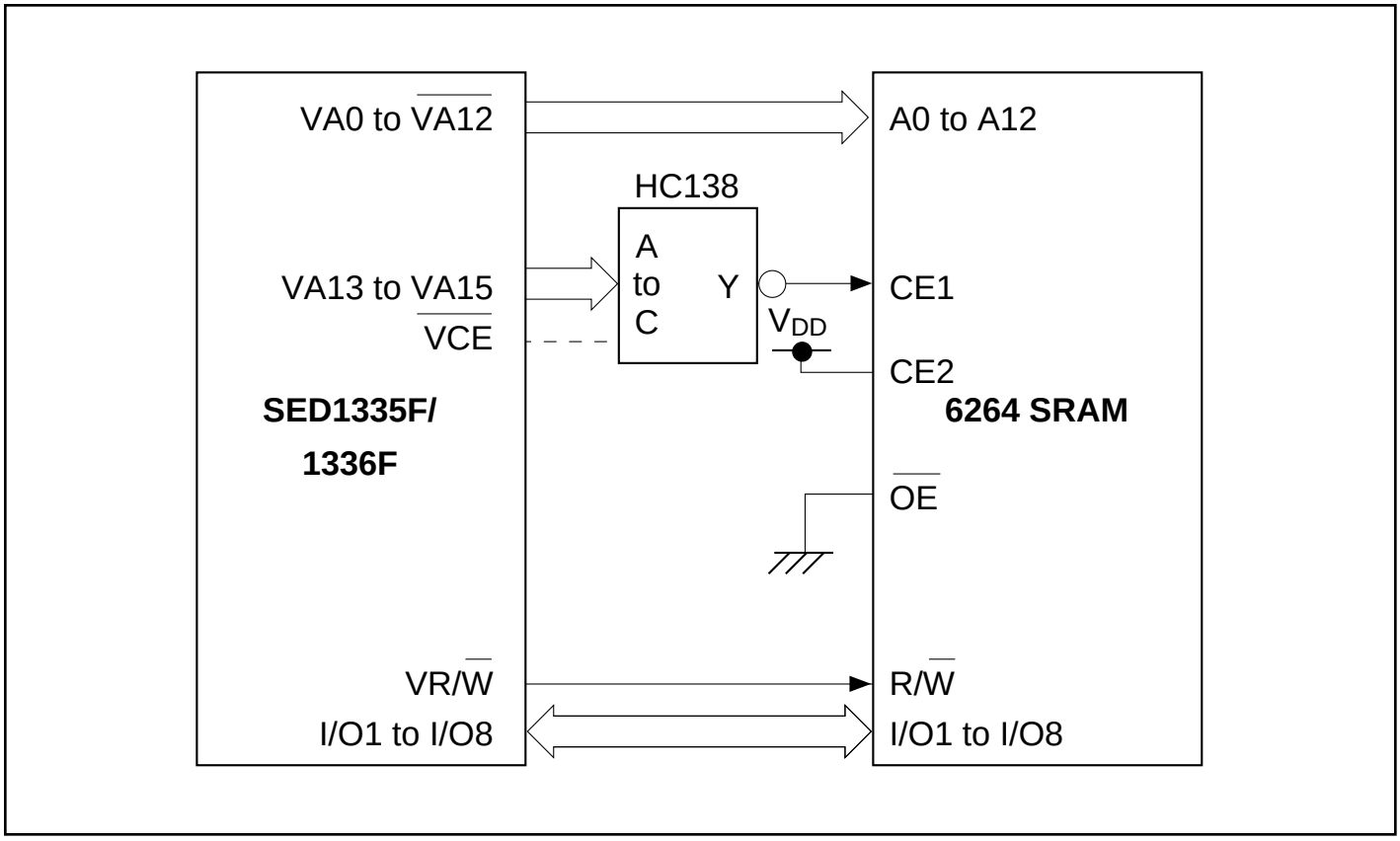


Figure 74. Static RAM interface

8.2.2 Supply Current during Display Memory Access

The 24 address and data lines of the SED1330F/1335F/1336F cycle at one-third of the oscillator frequency, f_{OSC}. The charge and discharge current on these pins, I_{VOP}, is given by the equation below. When I_{VOP} exceeds I_{OPR}, it can be estimated by:

$$I_{VOP} \propto C\ V\ f$$

where C is the capacitance of the display memory bus, V is the operating voltage, and f is the operating frequency.

If V_{OPR} = 5.0V, f = 1.0 MHz, and the display memory bus capacitance is 1.0 pF per line:

$$I_{VOP} \leq 120\ \mu A\ /\ MHz \times pF$$

To reduce current flow during display memory accesses, it is important to use low-power memory, and to minimize both the number of devices and the parasitic capacitance.

8.3 Oscillator Circuit

The SED1330F/1335F/1336F incorporates an oscillator circuit. A stable oscillator can be constructed simply by connecting an AT-cut crystal and two capacitors to OSC1 and OSC2, as shown in the figure below. If the oscillator frequency is increased, C_D and C_G should be decreased proportionally.

Note that the circuit board lines to OSC1 and OSC2 must be as short as possible to prevent wiring capacitance from changing the oscillator frequency or increasing the power consumption.

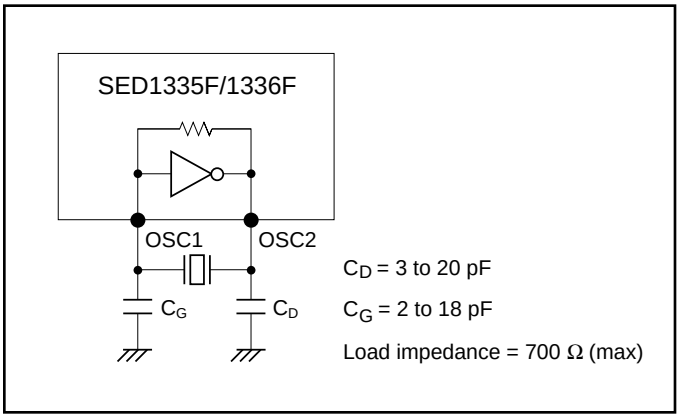


Figure 75. Crystal oscillator

8.4 Status Flag

The SED1330F/1335F/1336F has a single bit status flag.

D6: X line standby

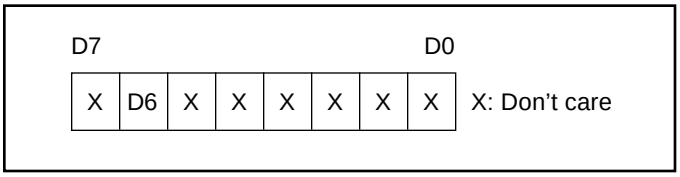


Figure 76. Status flag

The D6 status flag is LOW (0) for the TC/R - C/R cycles at the end of each line where the SED1330F/1335F/1336F is not reading the display memory. The microprocessor may use this period to update display memory without affecting the display; however, it is recommended that the display be turned off when refreshing the whole display.

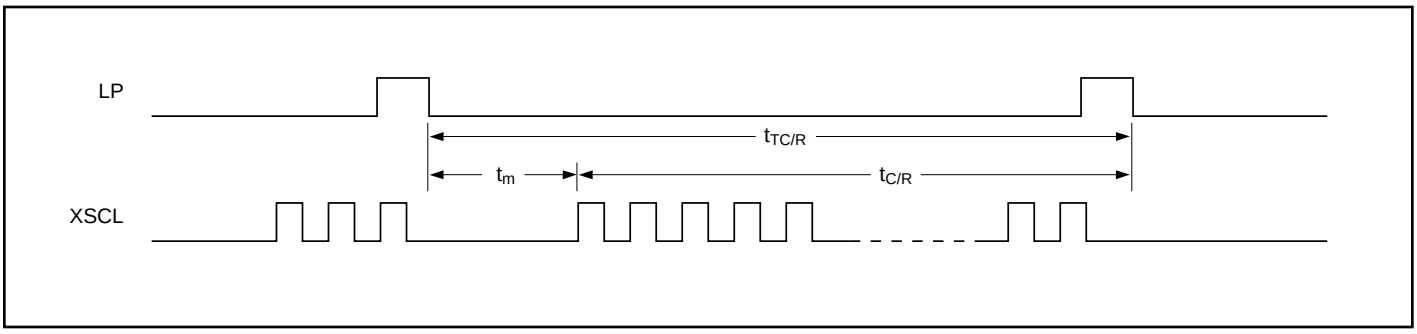


Figure 77. C/R to TC/R time difference

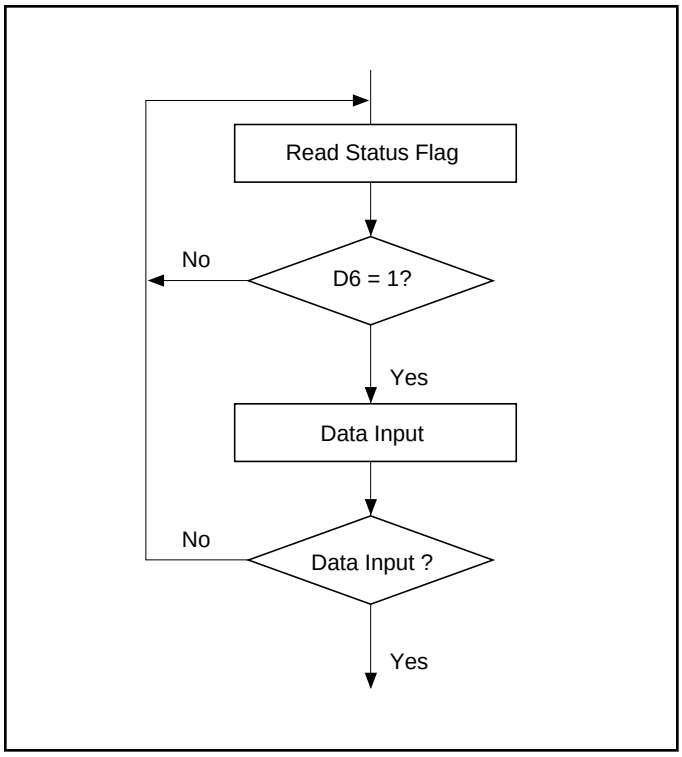


Figure 78. Flowchart for busy flag checking

8.5 Reset

The SED1330F requires a reset pulse at least 1 ms long after power-on in order to re-initialize its internal state. The SED1335F/1336F requires a minimum reset pulse of 200µs.

During reset, the LCD drive signals XD, LP and FR are halted.

For maximum reliability, it is not recommended to apply a DC voltage to the LCD panel while the SED1330F/1335F/1336F is reset. Turn off the LCD power supplies for at least one frame period after the start of the reset pulse.

The SED1330F/1335F/1336F cannot receive commands while it is reset. Commands to initialize the internal registers should be issued soon after a reset.

A delay of 3 ms (maximum) is required following the rising edges of both RES and V_{DD} to allow for system stabilization.

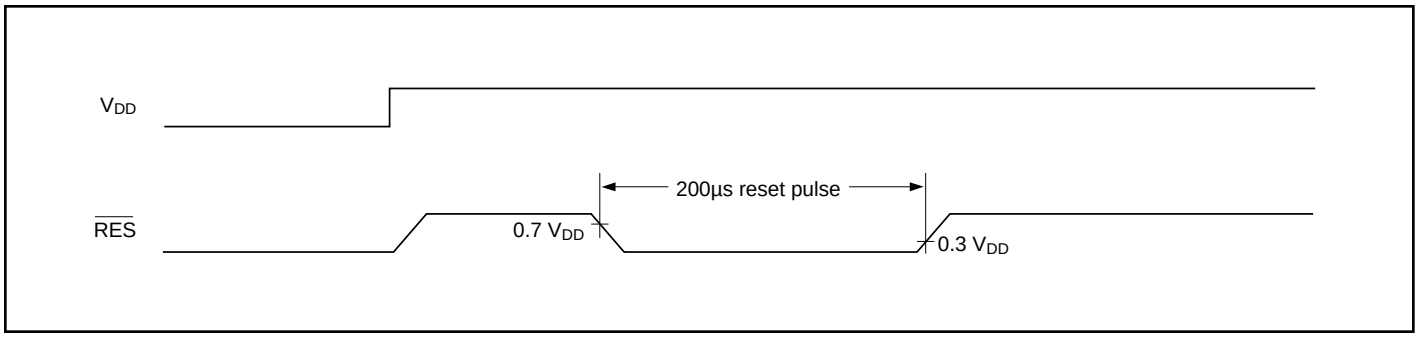


Figure 79. Reset timing

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9.0
Application Notes

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9.0 Application Notes

9.1 Initialization Parameters

The parameters for the initialization commands must be determined first. Square brackets around a parameter name indicate the number represented by the parameter, rather than the value written to the parameter register. For example, [FX] = FX + 1.

9.1.1 SYSTEM SET Instruction and Parameters

- **FX**

  The horizontal character field size is determined from the horizontal display size in pixels [VD] and the number of characters per line [VC].

  $[VD] / [VC] \leq [FX]$

  VD: # of X-directional dots
  VC: # of X-directional characters

- **C/R**

  C/R can be determined from VC and FX.

  $[C/R] = RND([FX] / 8) \times [VC]$

  where RND(x) denotes x rounded up to the next highest integer. [C/R] is the number of bytes per line, not the number of characters.

- **TC/R**

  TC/R must satisfy the condition [TC/R] ≥ [C/R] + 4.

- **f_{OSC} and f_{FR}**

  Once TC/R has been set, the frame frequency, f_{FR}, and lines per frame [L/F] will also have been set. The lower limit on the oscillator frequency f_{OSC} is given by:

  $$f_{OSC} \geq ([TC/R] \times 9 + 1) \times [L/F] \times f_{FR}$$

- If no standard crystal close to the calculated value of f_{OSC} exists, a higher frequency crystal can be used and the value of TC/R revised using the above equation.

- Symptoms of an incorrect TC/R setting are listed below. If any of these appears, check the value of TC/R and modify it if necessary.
  - Vertical scanning halts and a high-contrast horizontal line appears.
  - All pixels are on or off.
  - The LP output signal is absent or corrupted.
  - The display is unstable.

Table 31. Epson LCD unit example parameters (SED1335F only)

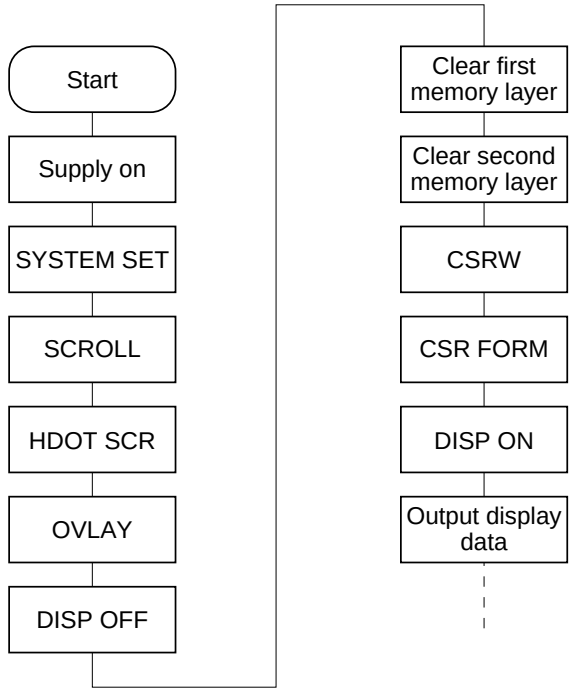
Resolution (X × Y)	[FX]	[FY]	[C/R]	TC/R	f_{OSC} (MHz) See Note 2
256 × 64	[FX] = 6 pixels: 256 / 6 = 42 remainder 4 = 4 blank pixels	8 or 16, depending on the screen	[C/R] = 42 = 2AH bytes: C/R = 29H. When using HDOT SCR, [C/R] = 43 bytes	2DH	1.85
512 × 64	[FX] = 6 pixels: 512 / 6 = 85 remainder 2 = 2 blank pixels	8 or 16, depending on the screen	[C/R] = 85 = 55H bytes: C/R = 54H. When using HDOT SCR, [C/R] = 86 bytes	58H	3.59
256 × 128	[FX] = 8 pixels: 256 / 8 = 32 remainder 0 = no blank pixels	8 or 16, depending on the screen	[C/R] = 32 = 20H bytes: C/R = 19H. When using HDOT SCR, [C/R] = 33 bytes	22H	2.90
512 × 128	[FX] = 10 pixels: 512 / 10 = 51 remainder 2 = 2 blank pixels	8 or 16, depending on the screen	[C/R] = 102 = 66H bytes: C/R = 65H. When using HDOT SCR, [C/R] = 103 bytes	69H	8.55

Notes:

1. The remainder pixels on the right-hand side of the display are automatically blanked by the SED1335F. There is no need to zero the display memory corresponding to these pixels.
2. Assuming a frame frequency of 60 Hz.

9.1.2 Initialization Example

The initialization example shown in Figure 80 is for a SED1330F/1335F/1336F with an 8-bit microprocessor interface bus display unit (512 × 128 pixels).



Note: Set the cursor address to the start of each screen's layer memory, and use MWRITE to fill the memory with space characters, 20H (text screen only) or 00H (graphics screen only). Determining which memory to clear is explained in section 9.1.3.

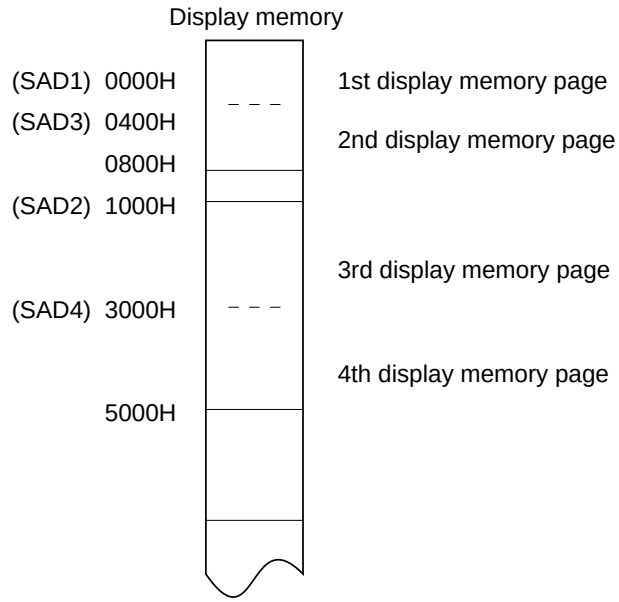
Figure 80. Initialization procedure

Table 32. Initialization procedure

No.	Command	Operation
1	Power-up	
2	Supply	Wait for at least 3 ms after reset with $V_{DD} \geq 4.5V$
3	SYSTEM SET	initialization.
	C = 40H	
	P1 = 38H	M0: Internal CG ROM M1: CG RAM is 32 characters maximum M2: 8 lines per character W/S: Two-panel drive IV: No top-line compensation
	P2 = 87H	FX: Horizontal character size = 8 pixels WF: Two-frame AC drive
	P3 = 07H	FY: Vertical character size = 8 pixels
	P4 = 3FH	C/R: 64 display addresses per line
	P5 = 49H	TC/R: Total address range per line = 90 f_{OSC} = 6.0 MHz, f_{FR} = 70 Hz
	P6 = 7FH	L/F: 128 display lines
	P7 = 80H	AP: Virtual screen horizontal size is 128 addresses
	P8 = 00H	
4	SCROLL	
	C = 44H	
	P1 = 00H	First screen block start address
	P2 = 00H	Set to 0000H
	P3 = 40H	Display lines in first screen block = 64
	P4 = 00H	Second screen block start address
	P5 = 10H	Set to 1000H
	P6 = 40H	Display lines in second screen block = 64
	P7 = 00H	Third screen block start address
	P8 = 04H	Set to 0400H

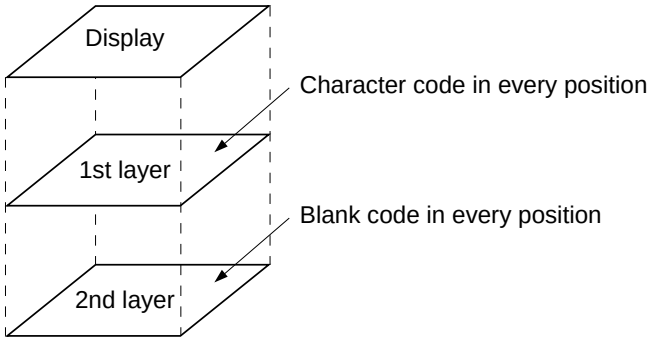
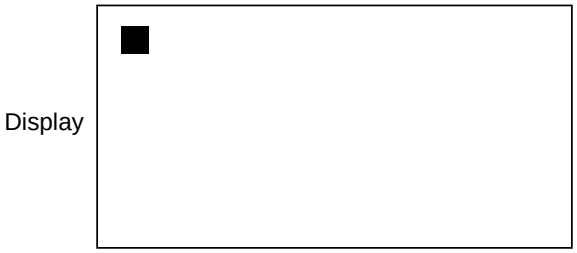
(continued)

Table 32. Initialization procedure (continued)

No.	Command	Operation
	P9 = 00H	Fourth screen block start address
	P10 = 30H	Set to 3000H
		
5	HDOT SCR	
	C = 5AH	
	P1 = 00H	Set horizontal pixel shift to zero
6	OVLAY	
	C = 5BH	
	P1 = 01H	MX 1, MX 0: Inverse video superposition DM 1: First screen block is text mode DM 2: Third screen block is text mode
7	DISP ON/OFF	
	C = 58H	D: Display OFF
	P1 = 56H	FC1, FC0: Flash cursor at 2 Hz FP1, FP0: First screen block ON FP3, FP2: Second and fourth screen blocks ON FP5, FP4: Third screen block ON
8	Clear data in first layer	Fill first screen layer memory with 20H (space character)

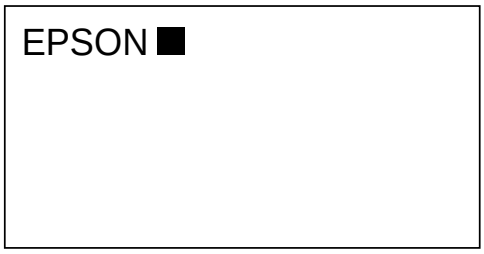
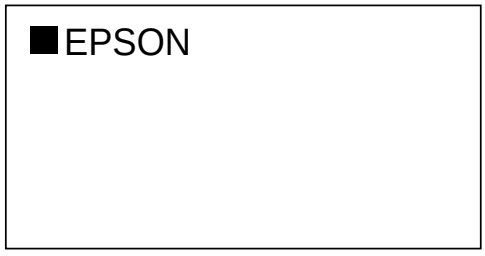
(continued)

Table 32. Initialization procedure (continued)

No.	Command	Operation
9	Clear data in second layer	Fill second screen layer memory with 00H (blank data) 
10	CSRW C = 46H P1 = 00H P2 = 00H	Set cursor to start of first screen block
11	CSR FORM C = 5DH P1 = 04H P2 = 86H	CRX: Horizontal cursor size = 5 pixels CRY: Vertical cursor size = 7 pixels CM: Block cursor
12	DISP ON/OFF C = 59H	Display ON 
13	CSR DIR C = 4CH	Set cursor shift direction to right

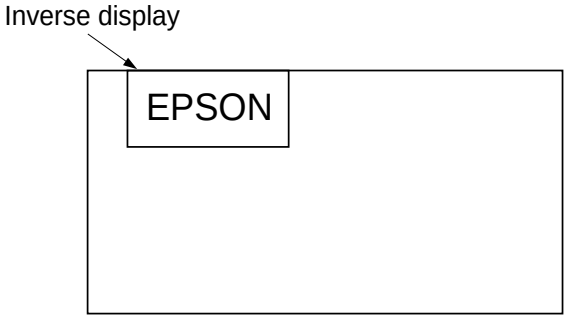
(continued)

Table 32. Initialization procedure (continued)

No.	Command	Operation
14	MWRITE	
	C = 42H	
	P1 = 20H	‘ ’
	P2 = 45H	‘E’
	P3 = 50H	‘P’
	P4 = 53H	‘S’
	P5 = 4FH	‘O’
	P6 = 4EH	‘N’
		
15	CSRW	
	C = 46H	
	P1 = 00H P2 = 10H	Set cursor to start of second screen block
16	CSR DIR	
	C = 4FH	Set cursor shift direction to down
17	MWRITE	
	C = 42H	
	P1 = FFH ↓ P9 = FFH	Fill in a square to the left of the ‘E’
		
18	CSRW	
	C = 46H	
	P1 = 01H P2 = 10H	Set cursor address to 1001H
19	MWRITE	
	C = 42H	

(continued)

Table 32. Initialization procedure (continued)

No.	Command	Operation
	P1 = FFH	Fill in the second screen block in the second column of line 1
	↓	
	P9 = FFH	
20	CSRW	Repeat operations 18 and 19 to fill in the background under 'EPSON'
↓		
29	MWRITE	
30	CSRW	
	C = 46H	
	P1 = 00H	Set cursor to line three of the first screen block
	P2 = 01H	
31	CSR DIR	
	C = 4CH	Set cursor shift direction to right
32	MWRITE	
	C = 42H	
	P1 = 44H	'D'
	P2 = 6FH	'o'
	P3 = 74H	't'
	P4 = 20H	' '
	P5 = 4DH	'M'
	P6 = 61H	'a'
	P7 = 74H	't'
	P8 = 72H	'r'
	P9 = 69H	'i'
	P10 = 78H	'x'
	P11 = 20H	' '
	P12 = 4CH	'L'
	P13 = 43H	'C'
	P14 = 44H	'D'

9.1.3 Display Mode Setting Example 1: Combining Text and Graphics

- **Conditions**
  - 320 × 200 pixels, single-panel drive (1/200 duty cycle)
  - First layer: text display
  - Second layer: graphics display
  - 8 × 8-pixel character font
  - CG RAM not required
- **Display memory allocation**
  - First layer (text): 320/8 = 40 characters per line, 200/8 = 25 lines. Required memory size = 40 × 25 = 1000 bytes.
  - Second layer (graphics): 320/8 = 40 characters per line, 200/1 = 200 lines. Required memory size = 40 × 200 = 8000 bytes.

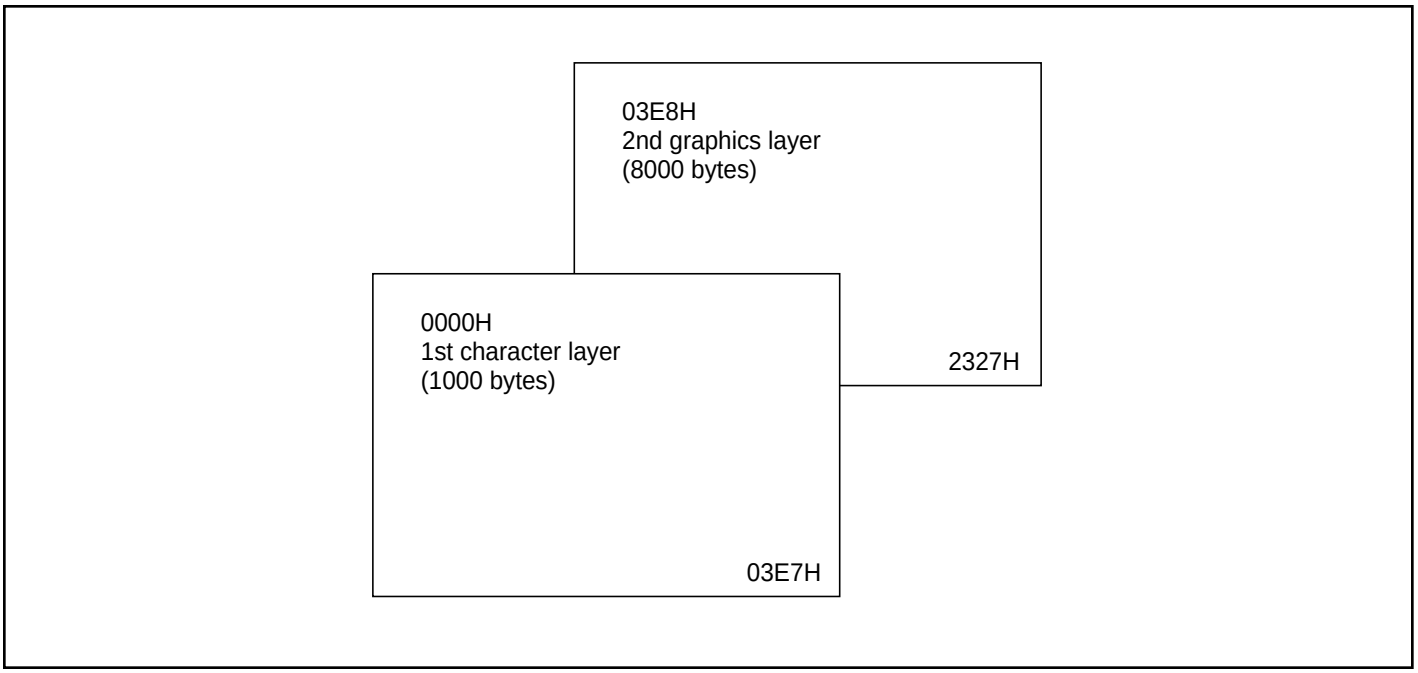


Figure 81. Character over graphics layers

- **Register setup procedure**

SYSTEM SET		TC/R calculation
C =	40H	
P1 =	30H	f_{OSC} = 6 MHz
P2 =	87H	f_{FR} = 70 Hz
P3 =	07H	
P4 =	27H	(1/6) × 9 × [TC/R] × 200 = 1/70
P5 =	2FH	[TC/R] = 48, so TC/R = 2FH
P6 =	C7H	
P7 =	28H	
P8 =	00H	

SCROLL	
C =	44H
P1 =	00H
P2 =	00H
P3 =	C8H
P4 =	E8H
P5 =	03H
P6 =	C8H
P7 =	XH
P8 =	XH
P9 =	XH
P10 =	XH

CSR FORM

C = 5DH

P1 = 04H

P2 = 86H

HDOT SCR

C = 5AH

P1 = 00H

OVLAY

C = 5BH

P1 = 00H

DISP ON/OFF

C = 59H

P1 = 16H

X = Don't care

9.1.4 Display Mode Setting Example 2: Combining Graphics and Graphics

- **Conditions**
  - 320 × 200 pixels, single-panel drive (1/200 duty cycle)
  - First layer: graphics display
  - Second layer: graphics display
- **Display memory allocation**
  - First layer (graphics): 320/8 = 40 characters per line, 200/1 = 200 lines. Required memory size = 40 × 200 = 8000 bytes.
  - Second layer (graphics): 320/8 = 40 characters per line, 200/1 = 200 lines. Required memory size = 8000 bytes.

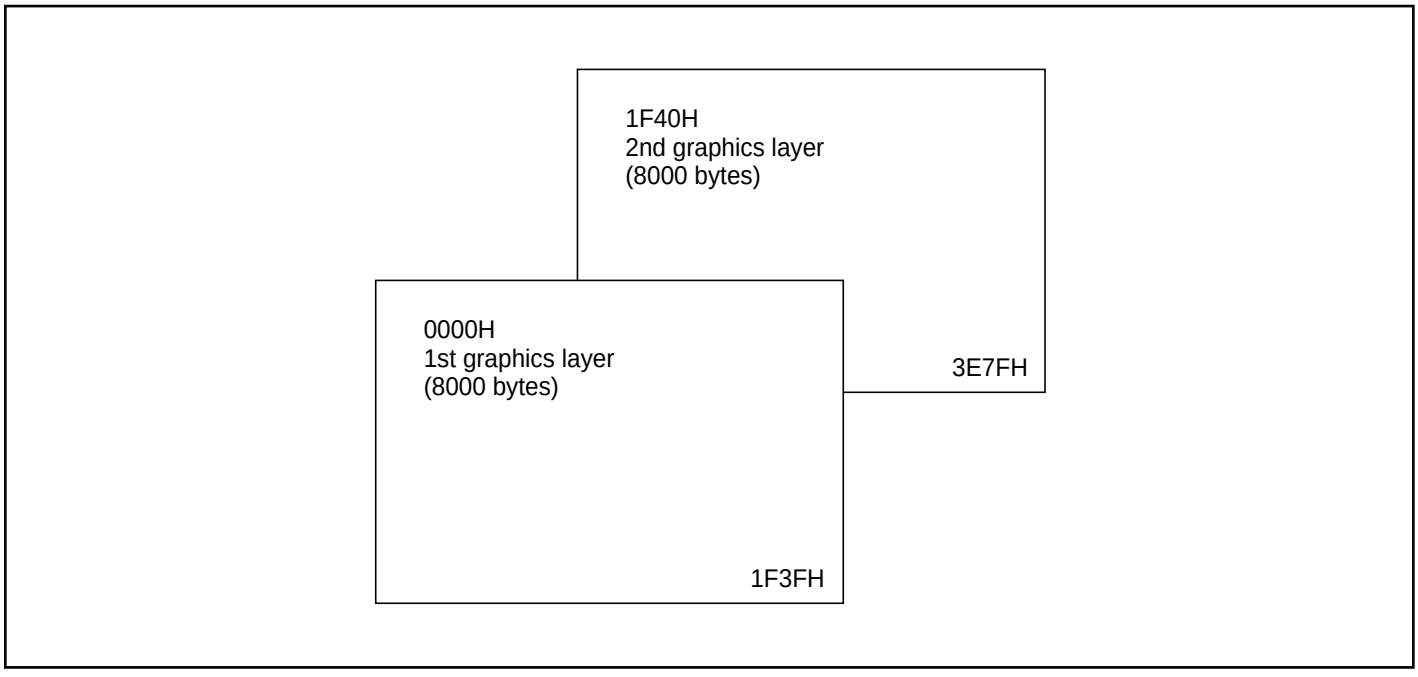


Figure 82. Two-layer graphics

- **Register setup procedure**

SYSTEM SET		TC/R calculation
C =	40H	
P1 =	30H	f_{OSC} = 6 MHz
P2 =	87H	f_{FR} = 70 Hz
P3 =	07H	
P4 =	27H	$(1/6)\times 9\times[TC/R]\times 200 = 1/70$
P5 =	2FH	[TC/R] = 48, so TC/R = 2FH
P6 =	C7H	
P7 =	28H	
P8 =	00H	

SCROLL	
C =	44H
P1 =	00H
P2 =	00H
P3 =	C8H
P4 =	40H
P5 =	1FH
P6 =	C8H
P7 =	XH
P8 =	XH
P9 =	XH
P10 =	XH

CSR FORM	
C =	5DH
P1 =	07H
P2 =	87H

HDOT SCR	
C =	5AH
P1 =	00H

OVLAY	
C =	5BH
P1 =	0CH

DISP ON/OFF	
C =	59H
P1 =	16H

X = Don’t care

9.1.5 Display Mode Setting Example 3: Combining Three Graphics Layers

- **Conditions**
  - 320 × 200 pixels, single-panel drive (1/200 duty cycle)
  - First layer: graphics display
  - Second layer: graphics display
  - Third layer: graphics display
- **Display memory allocation**
  - All layers (graphics): 320/8 = 40 characters per line, 200/1 = 200 lines. Required memory size = 40 × 200 = 8000 bytes.

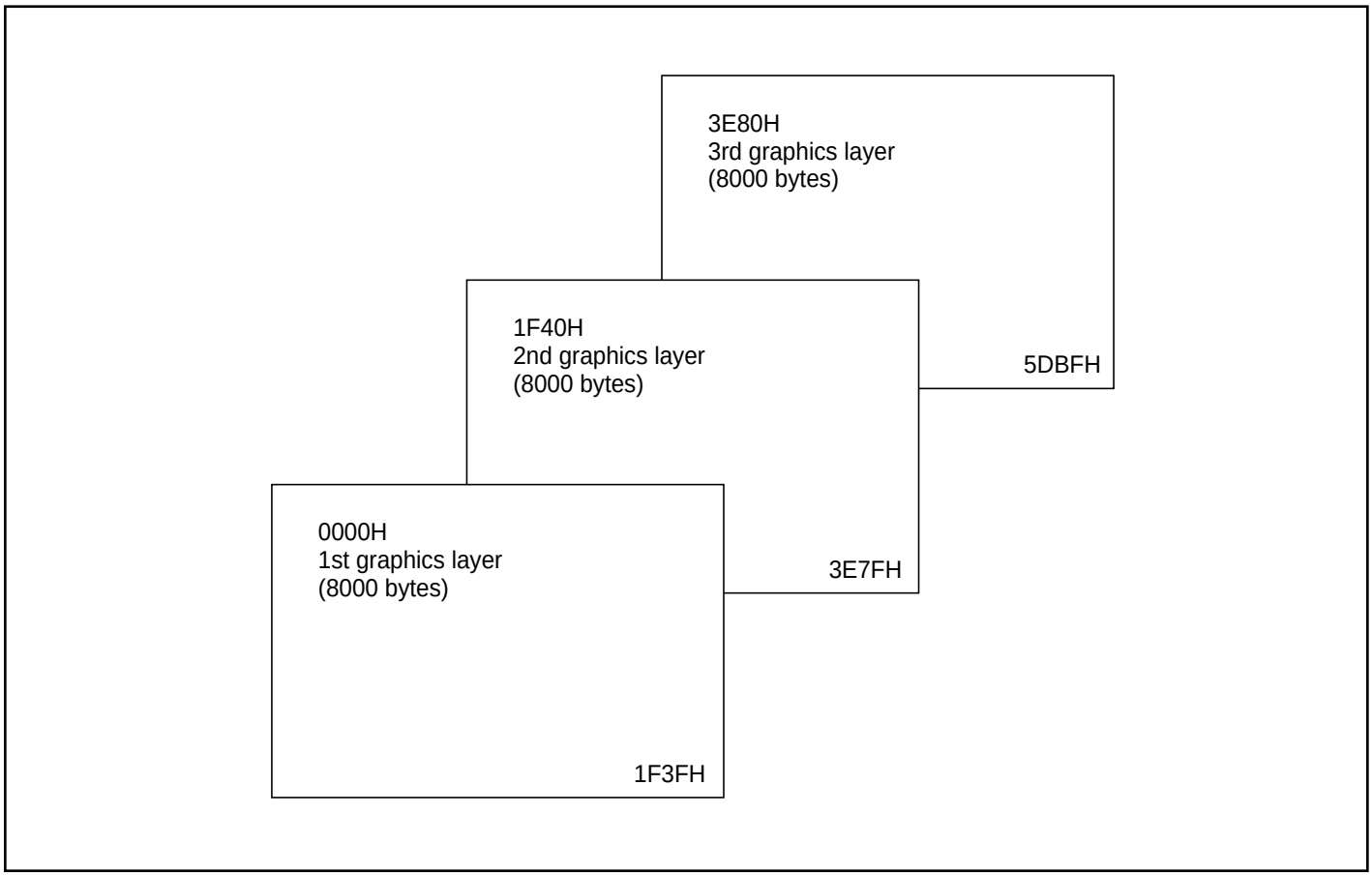


Figure 83. Three-layer graphics

- **Register setup procedure**

SYSTEM SET		TC/R calculation
C =	40H	
P1 =	30H	f_{OSC} = 6 MHz
P2 =	87H	f_{FR} = 70 Hz
P3 =	07H	
P4 =	27H	$(1/6)\times 9\times[TC/R]\times 200 = 1/70$
P5 =	2FH	[TC/R] = 48, so TC/R = 2FH
P6 =	C7H	
P7 =	28H	
P8 =	00H	

SCROLL	
C =	44H
P1 =	00H
P2 =	00H
P3 =	C8H
P4 =	40H
P5 =	1FH
P6 =	C8H
P7 =	80H
P8 =	3EH
P9 =	XH
P10 =	XH

CSR FORM

C = 5DH

P1 = 07H

P2 = 87H

HDOT SCR

C = 5AH

P1 = 00H

OVLAY

C = 5BH

P1 = 1CH

DISP ON/OFF

C = 59H

P1 = 16H

X = Don't care

9.2 System Overview

Figure 84 shows the SED1330F/1335F/1336F in a typical system. The microprocessor issues instructions to the 1330F/SED1335F/1336F, and the SED1330F/1335F/1336F drives the LCD panel and may have up to 64Kbytes of display memory.

Since all of the LCD control circuits are integrated onto the SED1330F/1335F/1336F, few external components are required to construct a complete medium-resolution liquid crystal display.

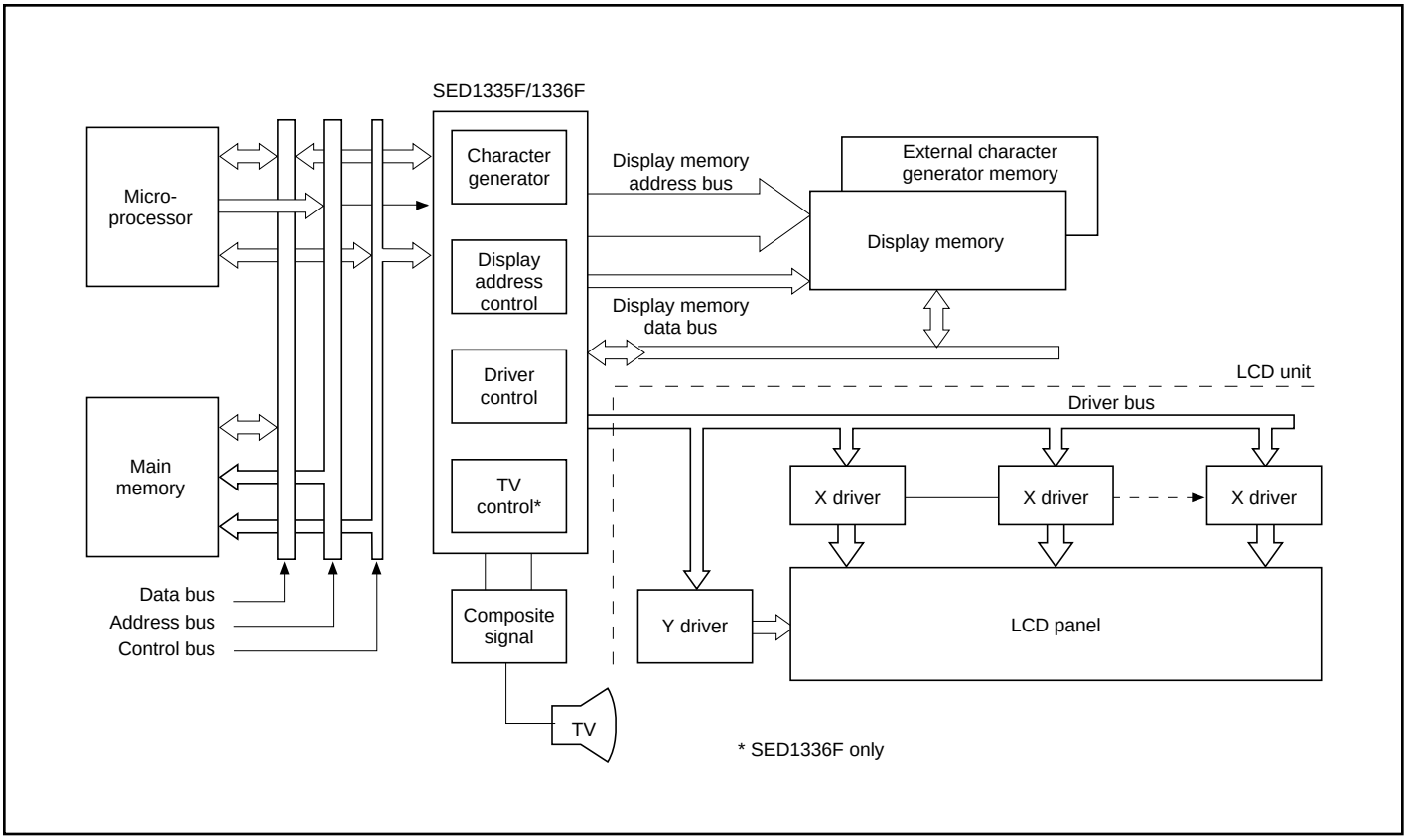
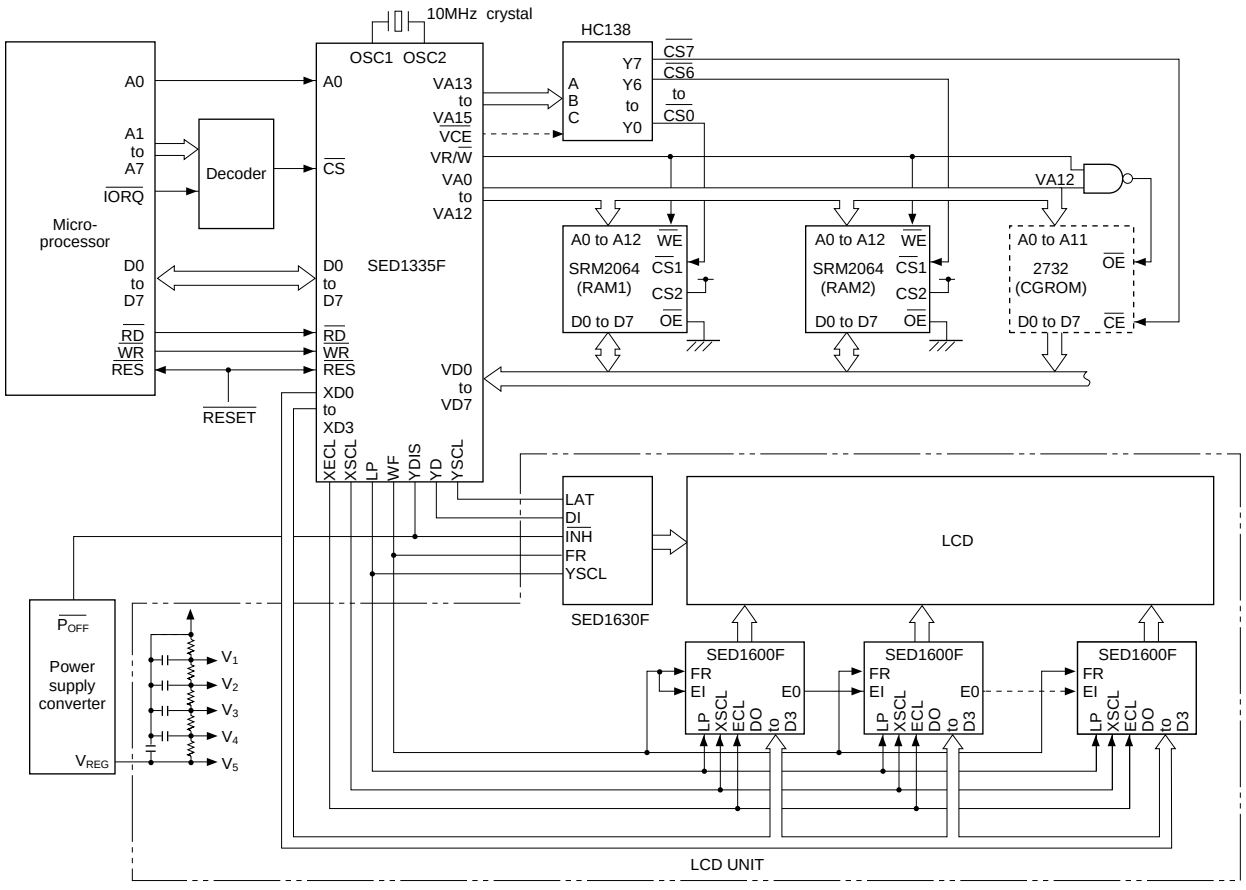


Figure 84. System block diagram

9.3 System Interconnection

9.3.1 SED1330F/1335F

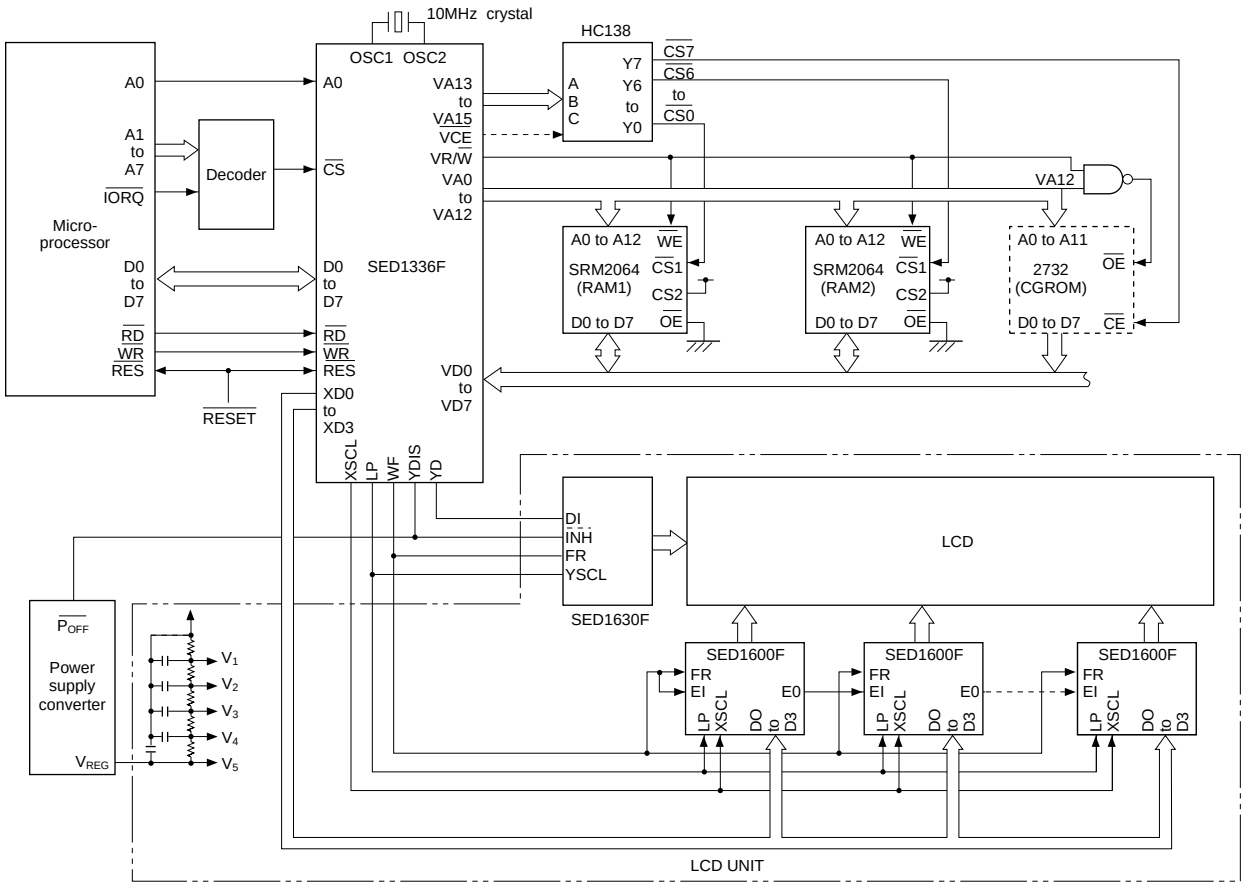


Notes:

1. The recommended common drivers are the SED1743, SED1635.
2. The recommended segment drivers are the SED1742 and SED1606.

Figure 85. System interconnection diagram

9.3.2 SED1336F



Notes:

1. The recommended common drivers are the SED1743, SED1635.
2. The recommended segment drivers are the SED1742 and SED1606.

Figure 86. System interconnection diagram

The SED1330F/1335F/1336F's layered screens and flexible scrolling facilities support a range of display functions and reduces the load on the controlling microprocessor when displaying underlining, inverse display, text overlaid on graphics or simple animation.

These facilities are supported by the SED1330F/1335F/1336F's ability to divide display memory into up to four different areas.

- **Character code table**
  - Contains character codes for text display
  - Each character requires 8 bits
  - Table mapping can be changed by using the scroll start function

- **Graphics data table**
  - Contains graphics bitmaps
  - Word length is 8 bits
  - Table mapping can be changed

- **CG RAM table**
  - Character generator memory can be modified by the external microprocessor
  - Character sizes up to 8 × 16 pixels (16 bytes per character)
  - Maximum of 64 characters
  - Table mapping can be changed

- **CG ROM table**
  - Used when the internal character generator is not adequate
  - Can be used in conjunction with the internal character generator and external character generator RAM
  - Character sizes up to 8 × 16-pixels (16 bytes per character)
  - Maximum of 256 characters
  - Fixed mapping at F000H to FFFFH

9.4 Smooth Horizontal Scrolling

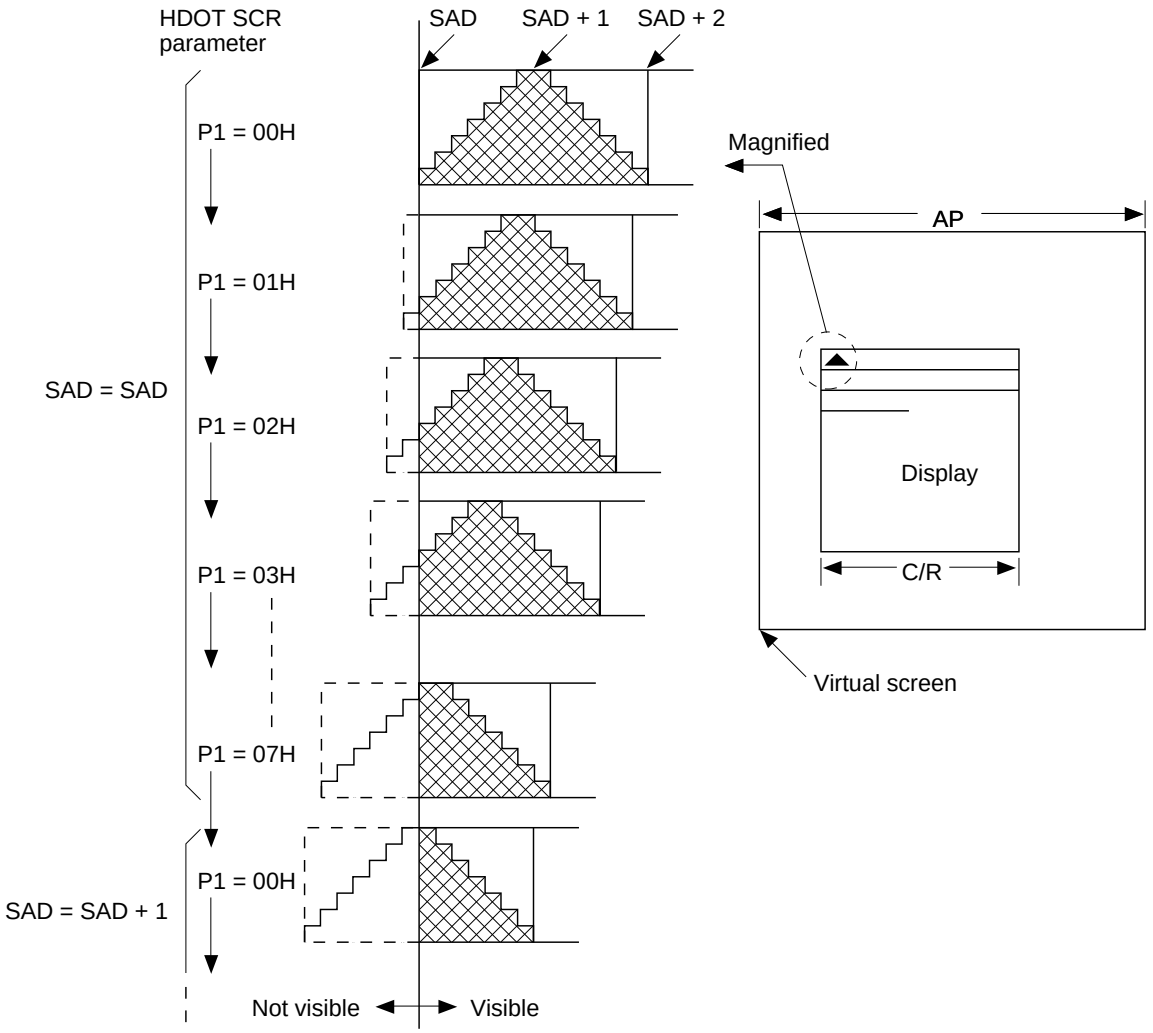
Figure 87 illustrates smooth display scrolling to the left. When scrolling left, the screen is effectively moving to the right, over the larger virtual screen.

Instead of changing the display start address SAD and shifting the display by eight pixels, smooth scrolling is achieved by repeatedly changing the pixel-shift parameter of the HDOT SCR command. When the display has been scrolled seven pixels, the HDOT SCR pixel-shift parameter is reset to zero and SAD incremented by one. Repeating this operation at a suitable rate gives the appearance of smooth scrolling.

To scroll the display to the right, the reverse procedure is followed.

When the edge of the virtual screen is reached, the microprocessor must take appropriate steps so that the display is not corrupted. The scroll must be stopped or the display modified.

Note that the HDOT SCR command cannot be used to scroll individual layers.



Note: The response time of LCD panels changes considerably at low temperatures. Smooth scrolling under these conditions may make the display difficult to read.

Figure 87. HDOT SCR example

9.5 Layered Display Attributes

SED1330F/1335F/1336F incorporates a number of functions for enhanced displays using monochrome LCD panels. It allows the display of inverse characters, half-intensity menu pads and flashing of selected screen areas. These functions are controlled by the OVLAY and DISP ON/OFF commands.

A number of means can be used to achieve these effects, depending on the display configuration. These are listed below. Note, however, that not all of these can be used in the one layer at the same time.

Attribute	MX1	MX0	Combined layer display	1st layer display	2ndt layer display
Reverse	0 1	1 1	IV EPSON	IV EPSON	
Half-tone	0 1	0 1	ME Yes, No	ME Yes, No	
Local flashing	0 0	0 1	BL Error	BL	Error
Ruled line	0 0 1	0 1 1	RL LINE LINE	RL LINE LINE	

Figure 88. Layer synthesis

9.5.1 Inverse Display

The first layer is text, the second layer is graphics.

1. CSRW, CSDIR, MWRITE

   Write 1s into the graphics screen at the area to be inverted.

2. OVLAY: MX0 = 1, MX1 = 0

   Set the combination of the two layers to Exclusive-OR.

3. DISP ON/OFF: FP0 = FP1 = 1, FP1 = FP3 = 0.

   Turn on layers 1 and 2.

9.5.2 Half-tone Display

The FP parameter can be used to generate half-intensity display by flashing the display at 17 Hz. Note that this mode of operation may cause flicker problems with certain LCD panels.

9.5.2.1 Menu Pad Display

Turn flashing off for the first layer, on at 17 Hz for the second layer, and combine the screens using the OR function.

1. OVLAY: P1 = 00H
2. DISP ON/OFF: P1 = 34H

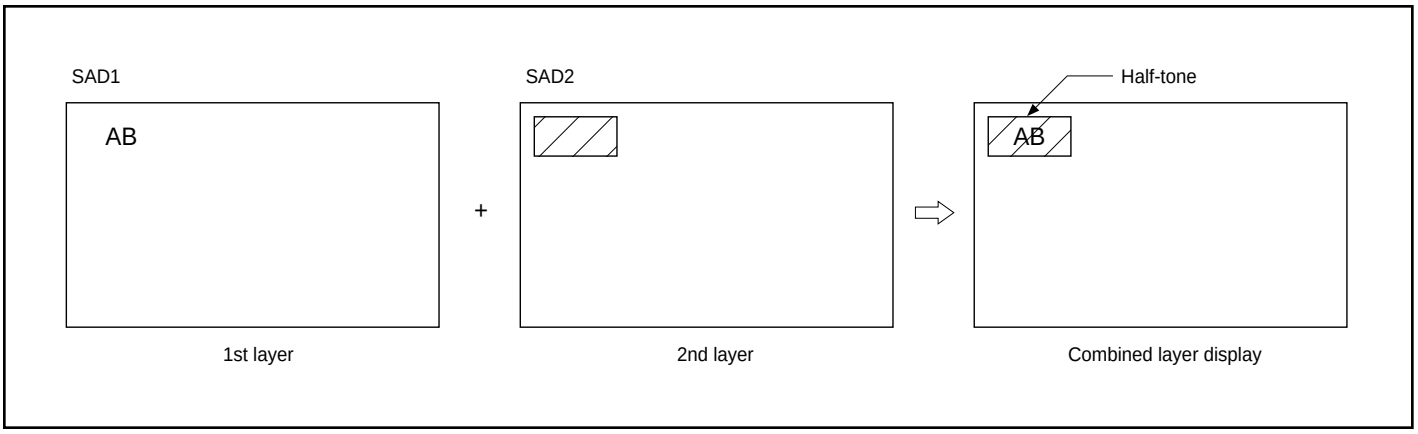


Figure 89. Half-tone character and graphics

9.5.2.2 Graph Display

To present two overlaid graphs on the screen, configure the display as for the menu bar display and put one graph on each screen layer. The difference in contrast between the half- and full-intensity displays will make it easy to distinguish between the two graphs and help create an attractive display.

1. OVLAY: P1 = 00H
2. DISP ON/OFF: P1 = 34H

9.5.3 Flashing Areas

9.5.3.1 Small Area

To flash selected characters, the MPU can alternately write the characters as character codes and blank characters at intervals of 0.5 to 1.0 seconds.

9.5.3.2 Large Area

Divide both layer 1 and layer 2 into two screen blocks each, layer 2 being divided into the area to be flashed and the remainder of the screen. Flash the layer 2 screen block at 2 Hz for the area to be flashed and combine the layers using the OR function.

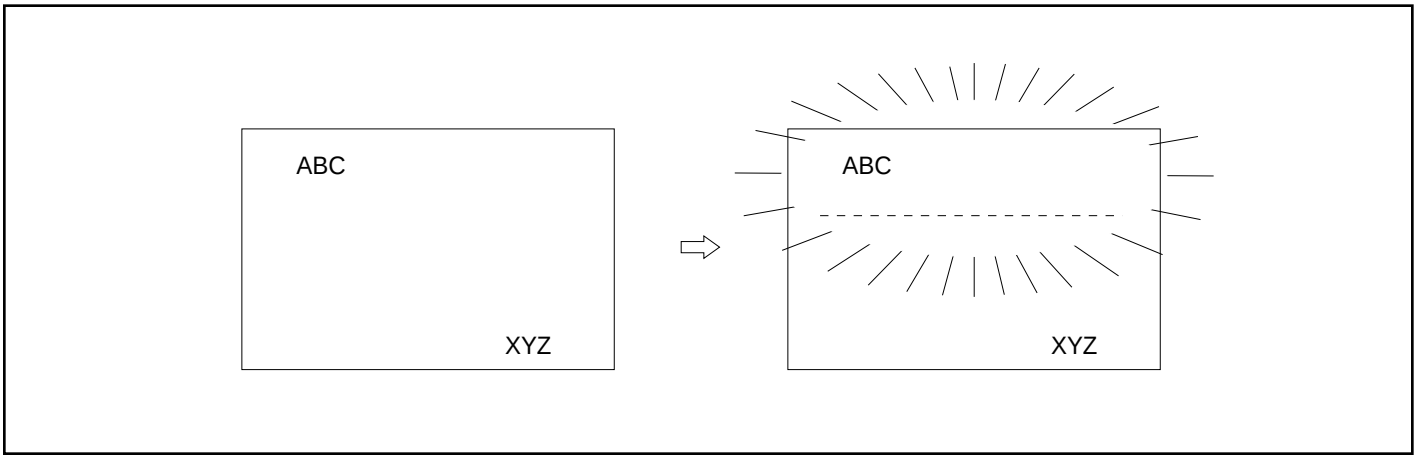


Figure 90. Localized flashing

9.6 16 × 16-dot Graphic Display

9.6.1 Command Usage

This example shows how to display 16 × 16-pixel characters. The command sequence is as follows:

CSRW Set the cursor address.

CSRDIR Set the cursor auto-increment direction.

MWRITE Write to the display memory.

9.6.2 Kanji Character Display

The program for writing large characters operates as follows:

1. The microprocessor reads the character data from its ROM.
2. The microprocessor sets the display address and writes to the VRAM. The flowchart is shown in Figure 91.

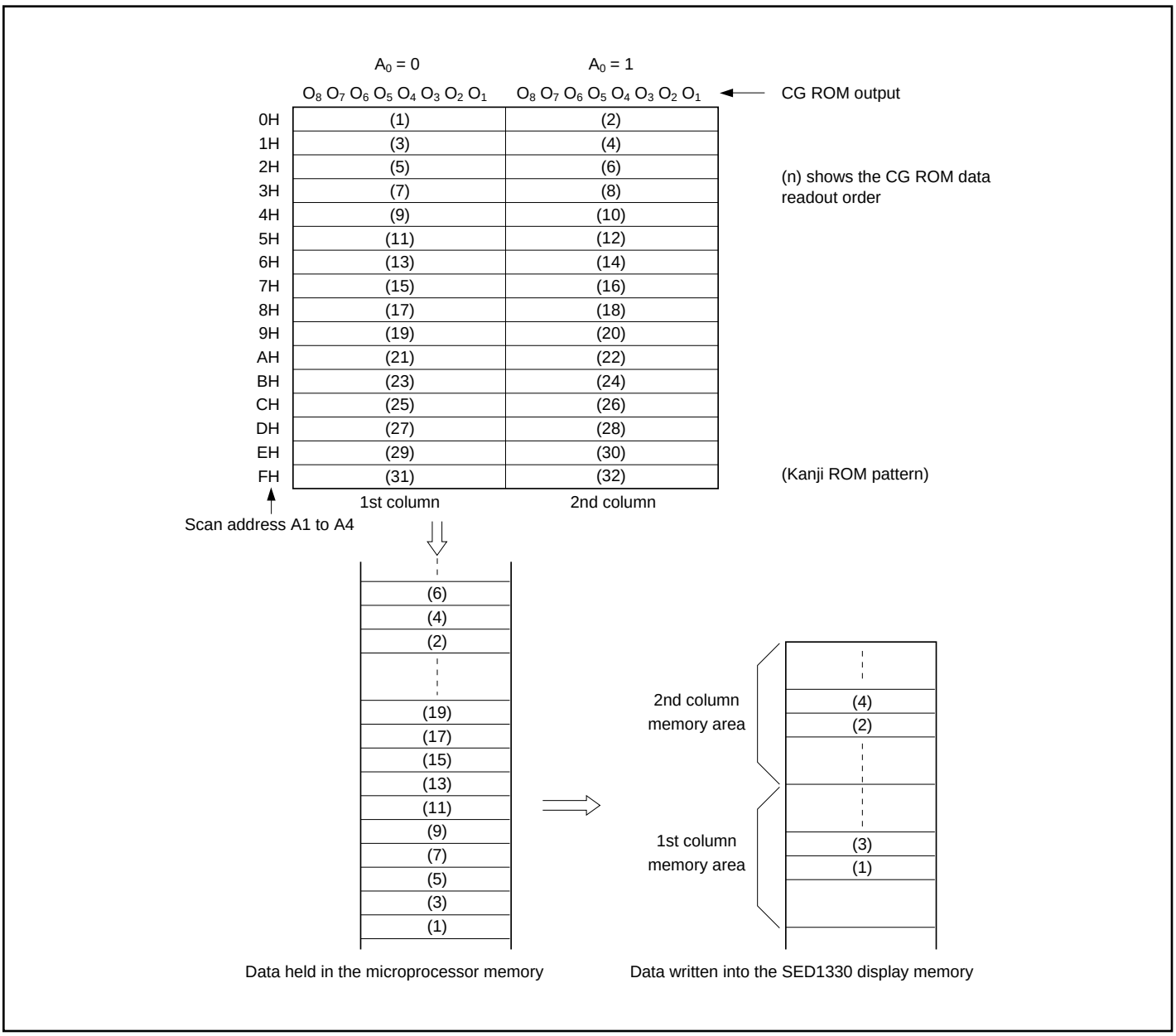


Figure 91. Graphics address indexing

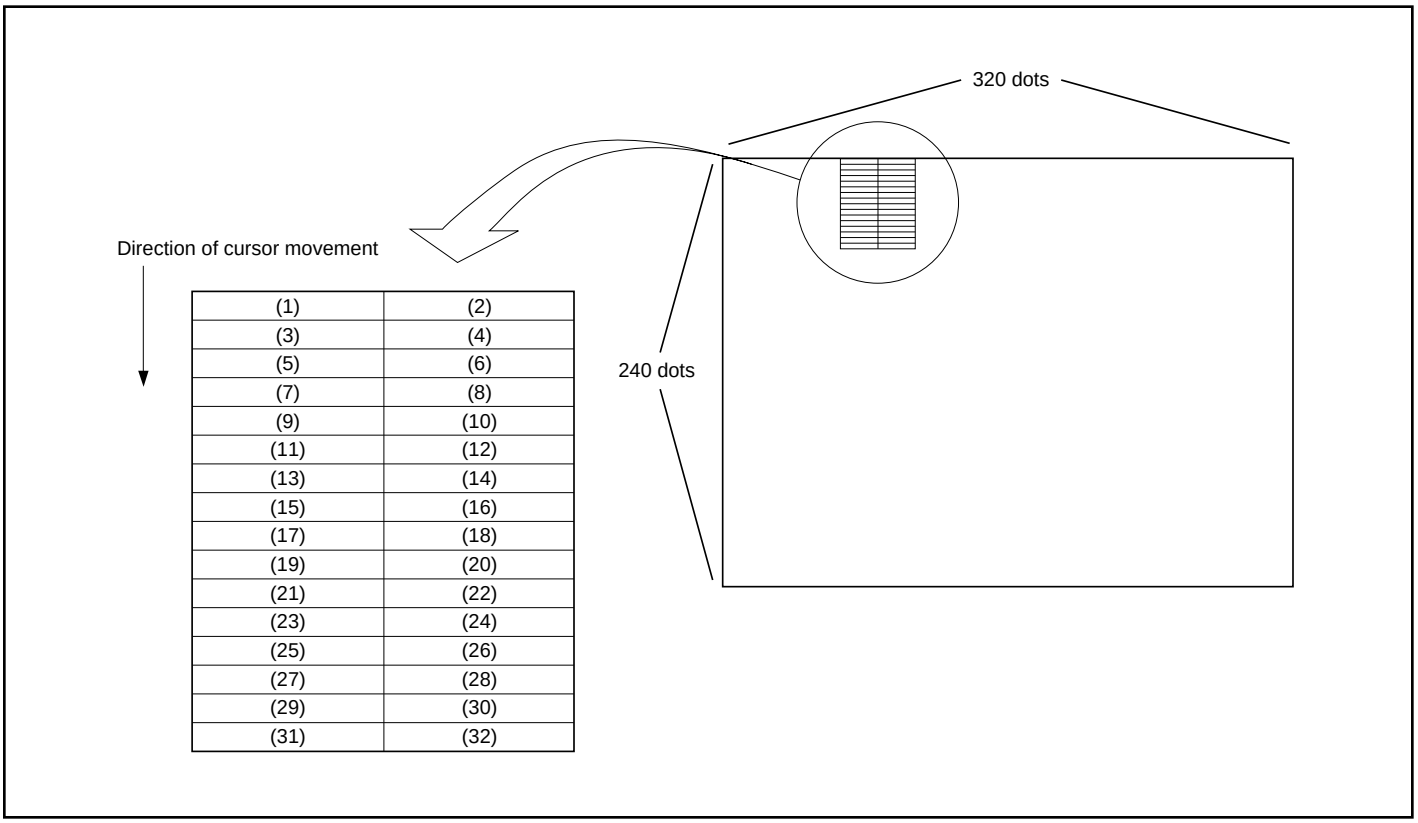


Figure 92. Graphics bit map

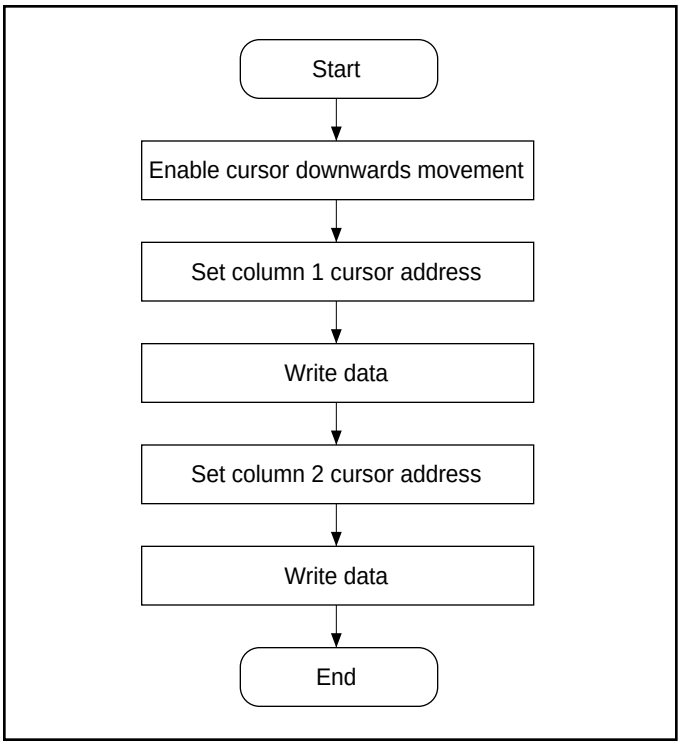


Figure 93. 16 × 16-dot display flowchart

Using an external character generator ROM, and 8 × 16-pixel font can be used, allowing a 16 × 16-pixel character to be displayed in two segments. The external CG ROM EPROM data format is described in Section 5.1. This will allow the display of up to 128, 16 × 16-pixel characters. If CG RAM is also used, 96 fixed characters and 32 bank-switchable characters can also be supported.

10.0
Internal Character Generator Font

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10.0 Internal Character Generator Font

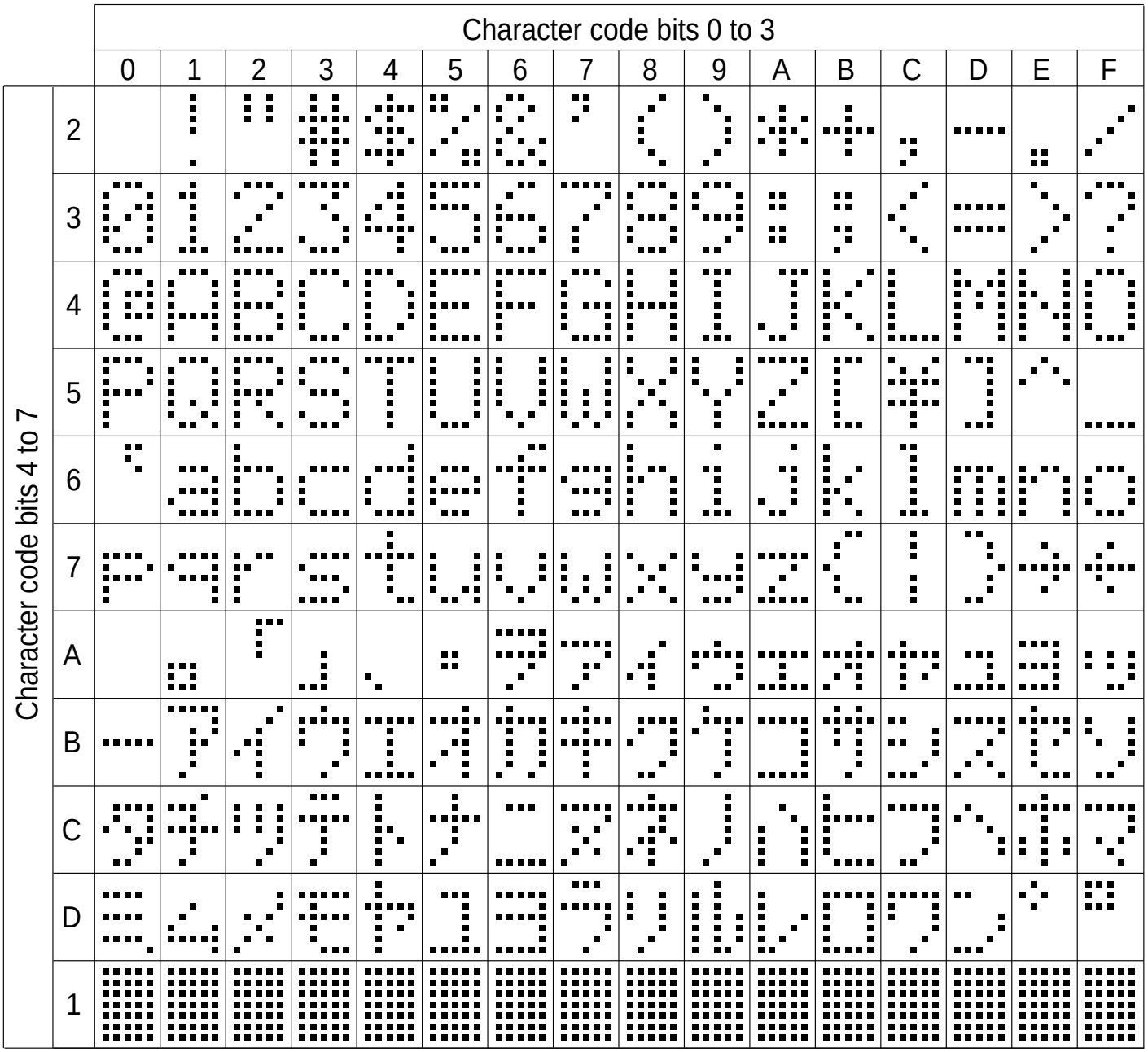

Figure 94. On-chip character set

Note: The shaded positions indicate characters that have the whole 6 × 8 bitmap blackened.

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11.0
Glossary of Terms

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11.0 Glossary of Terms

A	Address
AP	Address pitch parameter
C	Character display mode
CD	Cursor direction of movement parameter
CG	Character generator
CGRAM ADR	Character generator memory address
CM	Cursor display shape parameter
C/R	Characters per row parameter
CRX	Horizontal cursor size parameter
CRY	Vertical cursor size parameter
CSR DIR	Cursor direction of movement instruction
CSR FORM	Cursor size, position and type instruction
CSRR	Read cursor address register instruction
CSRW	Write cursor address register instruction
DM	Display mode parameter
FC	Flashing cursor parameter
f_{FR}	Frame frequency
f_{OSC}	Oscillator frequency
FP	Screen flashing parameter
FX	Horizontal character size parameter
FY	Vertical character size parameter
G	Graphics display mode
GLC	Graphic line control unit
HDOT SCR	Horizontal scrolling by pixels instruction
IV	Screen origin compensation for inverse display
L/F	Lines per frame instruction

MREAD	Display memory read instruction
MWRITE	Display memory write instruction
MX	Screen composition mode
OV	Graphics layer select parameter
OVLAY	Screen layer mode instruction
P	Parameter
R	Row
RAM	Random access memory
ROM	Read only memory
SAD	Display scrolling start address parameter
SL	Display scrolling length parameter
TC/R	Length, including horizontal blanking, of one screen line
VRAM	Display memory
WF	Display drive waveform parameter
W/S	Windows per screen parameter

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