A Flexible Common Language for Pocessor Hardware Description

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Abstract

Flexible Application Specific Instruction set Processors (ASIP) are starting to replace monolithic ASICs in a wide variety of fields. However the construction of an ASIP is today associated with a substantial design effort. NOGAP (Novel Generator of Micro Architectu and Processor) is a tool for ASIP designs utilizing hardware multiplexed data paths. One of the main advantages of NOGAP compared to other EDA tools for processor design, is that NOGAP impose few limits on the architecture and thus design freedom. NOGAP does not assume a fixed processor template and is not a data flow synthesizer. To reach this flexibility NOGAP makes heavy use of the compositional design principle. This paper describe NOGAPCL, a flexible common language for processor hardware descrpiton. A RISC processor using NOGAPCL has been constructed with NOGAP in less than a working day and synthesized to an FPGA. With no FPGA specific optimizations this processor met timing closure at 178MHz in a Virtex-4 LX80 speedgrade 12.