# Programmable Parallel Data-path for FEC

Rizwan Asghar, Dake Liu
Dept. of EE, Liinköpig University, SE-581 83 Linköping, Sweden
{rizwan, dake}  @isy.liu.se

## Abstract

We are trying to implement a flexible forward error correction (FEC) engine with programmability and re-configurability. The design focus is to provide a platform which supports maximum of the available algorithms (like Viterbi, Read Solomon, Turbo, LDPC, Interleaving and De-interleaving) as well as any newly evolved algorithm. The initial study presented in this paper will provide the basis for the evolution of the low cost hardware multiplexing of multiple FEC algorithms.