Very Low Cost Configurable Hardware Interleaver for 3G Turbo Decoding

Rizwan Asghar and Dake Liu
Department of Electrical Engineering, Linkoping university
Linkoping, Sweden
{rizwan, dake} @isy.liu.se

Abstract

A very low cost hardware interleaver for 3rd Generation Partnership Project (3GPP) turbo coding algorithm is presented. The interleaver is a key component of turbo codes and it is used to minimize the effect of burst errors in the transmission. Using conventional design methods, it consumes a large part of silicon area in the design of turbo encoder and decoder. The presented hardware interleaver architecture utilizes the algorithmic level hardware simplifications as well as the iterative modulo computation to achieve very low cost solution. After doing the hardware multiplexing and optimization the proposed architecture consumes only 1.5 k gates (without pre-computation) and 2.2 k gates (with precomputation). In both cases the interleaved address is computed every clock cycle except the case of pruning, in which one additional clock cycle is consumed.