Automatic Port and Bus Sizing in Novel Generator of Accelerators and Processors (NoGap)

Per Karlström, Wenbiao Zhou, Dake Liu
Division of Computer Engineering
Department of Electrical Engineering
E-mail: {perk, zhou,dake} @isy.liu.se

Abstract:

ASIP processors and programmable accelerators are replacing monolithic ASICs in more and more areas. However the design and implementation of a new ASIP processor or programmable accelerator requires a substantial design effort. There are a number of existing tools that promise to ease this design effort, but using these tools usually means that the designer get locked into the tools a~priori assumtions and it is therefore hard to develop truly novel ASIPs or accelerators. NoGAP is a tool that delivers design support while not locking the designer into any predefined template architecture. An important aspect of NoGAP's design process is the ability to design the data path of each instruction individually. Therefore the size of input/output ports can sometimes not be known while designing the individual functional units. For this reason we have introduced the concept of dynamic port sizes, which is an extension of the parameter/generic concept in Verilog/VHDL. A problem arises if the data path graph contains loops, either due to intra or inter instruction dependencies. This paper will present the algorithm used to solve this looping problem.