JOUST: a Uniform Approach for Processor Design in NoGAP

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Abstract

Flexible Application Specific Instruction set Processors (ASIP) are starting to replace monolithic ASICs in a wide variety of fields. However the construction of an ASIP is today associated with a substantial design effort. NoGAP (Novel Generator of Micro Architecture and Processor) is a tool for ASIP designs, utilizing hardware multiplexed data paths. One of the main advantages of NoGAP compared to other EDA tools for processor design, is that NoGAP imposes few limits on the architecture and thus design freedom. NoGAP does not assume a fixed processor template and is not a data flow synthesizer. To reach this flexibility NoGAP makes heavy use of the compositional design principle. This paper presents a new approach to deal with processor design. The new approach is named JOUST (Judgment and Operation Unified STructure), it is a unified way to describe control and data paths in NoGAP, the JOUST approach is a more favorable to construct complex processor. A RISC processor named PIONEER has been constructed with the proposed JOUST approach in NoGAP. It was constructed in about a work-week. It has also been synthesized and tested on an FPGA. With no FPGA specific optimizations, PIONEER processor meet timing closure at 203MHz in a Virtex-4 LX80 speedgrade 12.