# Design of SENIOR: a Case Study using NoGAP

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**Abstract**

ASIP are needed to handle the future demand of flexible yet high performance computation in mobile devices. The flexibility of ASIP makes them preferable over fixed function ASIC. Also, a well designed ASIP, has a power consumption comparable to ASIC. However the cost associated with ASIP design is a limiting factor for a more wide spread adoption. A number of different tools have been proposed, promising to ease this design process. However all of the current state of the art tools limits the designer due to a template based design process. We have therefore proposed the NoGAP. NoGAP is a design automation tool for ASIP design that puts very few limits on the designer, yet it supports a designer by automating much of the tedious and error prone tasks associated with ASIP design. This paper presents a case study, where we used NoGAP to redesign an advanced RISC processor, with DSP extensions, which is called SENIOR. The NoGAP generated System Verilog code was synthesized to both an FPGA and an ASIC flow. The design time needed to implement SENIOR using NoGAP was three man-weeks. With no FPGA specific optimizations, NoGAP SENIOR met timing closure at 85 MHz which is close to original SENIOR when targeted to a Virtex 4 LX80 speed-grade 12. The resulting maximum frequency for the ASIC design were 215 MHz, which is only 10% less than original SENIOR in 65nm technology with 100% low power logic cell. The resulting area and power consumption of the ASIC design was 577689 um2 and 2.5654 mW (estimated) respectively which are similar to the performance of the original design. Examining the critical paths we could conclude that hardware synthesize by NoGAP was not a limiting factor.