Operation Classification for Control Path Synthetization with NoGAP

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Abstract

Flexible Application Specific Instruction set Processors (ASIP) are starting to replace monolithic ASICs in a wide variety of fields. However the construction of an ASIP is today associated with a substantial design effort. NoGAP (Novel Generator of Micro Architecture and Processor) is a tool for ASIP designs utilizing hardware multiplexed data paths. One of the main advantages of NoGAP compared to other ADL tools is that it does not impose limits on the architecture and thus design freedom. NoGAP does not assume a fixed processor template and is not another data flow synthesizer. To reach this flexibility NoGAP makes heavy use of the compositional design principle and is therefore divided into three parts Mage, Mase, and Castle. This paper discusses the techniques used in NoGAP for control path synthetization. A RISC processor has been constructed with NoGAP in less than a working day and synthesized to an FPGA. With no FPGA specific optimizations this processor met timing closure at 178MHz in a Virtex-4 LX80 speedgrade 12.