A comparison of three FPGA optimized NoC architectures

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Abstract:

Networks on chip has long been seen as a possible solution to the on-chip interconnection problems encountered when dealing with large system on a chip designs. However, almost all network on chip publications are primarily targeting ASIC solutions. In this paper we instead describe the details of three different network types optimized for the Virtex-4 FPGA architecture; a packet switched, a circuit switched and a minimalistic network without arbitration. The latter is included primarily for performance comparisons. The networks have lower latency, smaller area, or higher clock frequency when compared to other FPGA based on-chip networks found in the literature.