Using Partial Reconfigurability to aid Debugging of FPGA Designs

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Abstract:

This paper discusses the use of partial reconfigurability in Xilinx FPGA designs in order to aid debugging. A debugging framework is proposed where the use of partial reconfigurability can allow for added flexibility by allowing a debugger to decide at run time what debugging module to use. This paper also presents an open source debugging tool which allows a user to read-out the contents of memory blocks in Xilinx designs without needing to use any JTAG adapter. This allows a user to debug an FPGA in situations which would otherwise be difficult, i.e. in the field.