PARALLELIZATION OF HIGH-PERFORMANCE VIDEO ENCODING ON A SINGLE-CHIP MULTIPROCESSOR

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Abstract

Although single-chip multiprocessor architectures are available nowadays for embedded computing, programming them with efficiency and productivity has become a significant challenge. This paper studies the multi-level parallelization of video encoding algorithms on a state-of-the-art onchip multiprocessor. The encoding of H.264/AVC video is chosen as the case to be studied because of its performance demanding and branch-rich features. The final benchmarking result proves that the optimized processing flow can achieve more than 100 operations per cycle in performance which allows a single-chip multiprocessor to encode high resolution video (1920 × 1080) in real-time (30 fps).