System Architecture for 3GPP LTE Modem using a Programmable Baseband Processor

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Abstract
3G evolution towards HSPA and LTE is ongoing which will substantially
increase the throughput with higher spectral efficiency. This paper presents the system
architecture of an LTE modem based on a programmable baseband processor. The
architecture includes a baseband processor that handles processing such as time and frequency
synchronization, IFFT/FFT (up to 2048-p), channel estimation and subcarrier demapping.
The throughput and latency requirements of a Category 4 User Equipment (CAT4 UE) is met
by adding a MIMO symbol detector and a parallel Turbo decoder supporting
H-ARQ. This brings both low silicon cost and enough flexibility to support
other wireless standards. The complexity demonstrated by the modem shows the practicality
and advantage of using programmable baseband processors for a single-chip LTE solution.