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*Implementation of A High-Speed Parallel Turbo Decoder for
3GPP LTE Terminals*

Abstract:

This paper presents a parameterized parallel Turbo decoder for 3GPP LTE terminals. To support the high peak data-rate defined in the forthcoming 3GPP LTE standard, Turbo decoder with a throughput beyond 150Mbit/s is needed as a key component of the radio baseband chip. By exploiting the tradeoff of precision, speed and area consumption, a Turbo decoder with eight parallel SISO units is implemented to meet the throughput requirement. The turbo decoder is synthesized, placed and routed using 65nm CMOS technology. It achieves a throughput of 152Mbit/s and occupies an area of 0.7mm² with estimated power consumption being 650mW .