Processor friendly peak-to-average reduction in multi-carrier systems

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Abstract

In this paper a computationally efficient method of reducing the peak-to-average ratio of an OFDM system is presented. Today there exist many excellent peak-to-average reduction schemes; they are however mainly focused on maximum peak reduction, not on moderate computation cost. The proposed method is based on a tradeoff between computation cost and peak reduction performance. The method is also compared to existing methods both in terms of average constellation error magnitude and cycle cost. We also propose a hardware accelerator scheme in order to further reduce the cycle cost. Simulations have shown a moderate 3-4 dB SNR degradation compared to common computation intensive methods which require up to 40 times more operations.

1 Introduction

One of the largest drawbacks of OFDM based modulation schemes is the inherent large peak to average ratio. Peaks in the output signal are inherent in all multi-carrier systems, especially in OFDM systems. These peaks will cause clipping in the power amplifier and thus reduce SNR and create out of band noise. Peak reduction is essential in order to relax the design constraints of the power amplifier and to avoid unnessecary power consumption in the amplifier stage.

However since most PAR reduction methods are so cycle consuming that they cannot be implemented using a programmable DSP a simplified method is presented.

The paper is organized as follows. In section 2, we give the background of peak-to-average reduction. In section 3, the principle of soft limiting is presented. In section 4, the proposed method is presented. In section 5 the results are presented. Finally, future work is discussed in section 6 and conclusions are drawn in section 7.

2 Background

The most important problem associated with OFDM systems is the inherent high peak-to-average ratio (PAR), which requires a highly linear power amplifier. When a power amplifier is subjected to a peak input, the inherit power limitation of the amplifier will limit, *clip*, the signal and thus both cause signal degradation by distortion and out-of-band noise (OBN). The peak-to-average ratio, ε, is defined by:

$$\varepsilon = \frac{max|x(t)|^2}{E[|x(t)|^2]}$$

The output signal created by the modulator in IEEE 802.11a is usually created by an inverse fast fourier transform using 52 out of 64 sub-carriers. The time-domain signal from the IFFT is described by:

$$x(t) = \frac{1}{\sqrt{N}} \sum_{n=0}^{N-1} X_n e^{j2\pi f_n t} \qquad N = 64$$

$$\max|X_n| = 1$$

The maximum peak amplitude is 52 times the amplitude of a single sub-carrier. The maximum peak case is created when all sub-carriers are added with the same sign. This maximum value is seldom reached, however peaks occur regularly.

One of the key parameters of power amplifiers which characterizes the response to peaks is the 1 dB compression point, i.e. the point where the amplification has fallen by 1 dB below the expected output power. See Figure 1.

When the input signal exceeds the linear region of the amplifier, distortion will be introduced. This

distortion has two effects, it will create spurious signals both in and out of the desired band of operation, and it will clip the amplitude of the transmitted signal and thus increase the bit error rate (BER).

Spurious signals out-of-band must also be kept to a minimum, as they can interfere with other communication equipment or systems.

In order to avoid saturating the power amplifier, the input signal must be reduced so most of the signal will fall within the linear region. This reduction is referred to as *back-off*, and must be chosen in such a way that possible peaks of the input signal won't fall within the non-linear region.

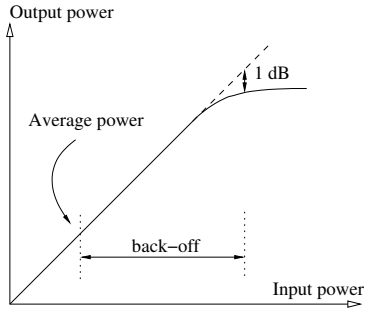

Figure 1: 1 dB compression point

However, increasing the back-off of a class-A power amplifier, severely reduces its efficiency. Standard class-A amplifier efficiency functions [1] yields a maximum efficiency of only ∼6.25%.

To ensure an undistorted signal with 20 mW (+13 dBm) average output power, about 320 mW of supply power is required with 9 dB back-off. This low efficiency is unacceptable in a mobile environment.

In order to ease the requirements on power amplifiers, and especially high power amplifiers, digital correction and peak reduction must be employed to lower the PAR.

3 Corrective algorithms

There are several methods of reducing PAR; however this paper will be focused on soft clipping.

The idea of soft clipping is to limit the signal amplitude before it reaches the power amplifier. If clipping is performed on the Nyquist-sampled signal (20 Msps[1]), all clipping noise will fall in-band and cause distortion. However if clipping is performed on an up-sampled signal, the noise will be distributed both in-band and out-of-band. Since the in-band noise cannot be filtered, it will degrade SNR and BER.

Common correction methods such as the one described in [3] function according to the following principle:

The result from the mapper is fed to an up-sampled IFFT and then clipped by a soft limiter. The clipped signal is then converted back to frequency domain by a down-sampling FFT and later corrected for phase and amplitude errors by a polar limiter. The corrected frequency domain representation of the signal is then converted back to a time domain signal by an IFFT and then fed to the transmitter. This is illustrated by Figure 2.

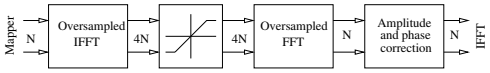

Figure 2: Soft clipping and correction.

The processing cost for this correction includes:

- 256 point IFFT. (4 ↑)
- Complex power limit on 256 samples.
- 256 point FFT. (4 ↓)
- Polar phase and amplitude correction (limit) on 64 samples.

The complex power limit of the interpolated time domain sequence can be realized by an iterative vector maximum search which returns the address to the largest element. This element is then scaled by a real valued scaling factor which maintains the phase information of the sample. By scaling the real and imaginary part of the time domain sample by the same factor, the phase of the signal is maintained. This scaling is referred to as polar scaling. Polar scaling will help to prevent spectrum and peak re-growth and thus lower the BER.

After the signal is converted back into frequency domain, the polar phase and amplitude correction step will ensure that the maximum amplitude and phase deviation from the desired constellation point is limited to a user defined value. The correction unit can of course not reset the sample value to the original constellation point since then the original peak would appear again.

One of the main challenges of the polar limit unit is the problem of converting rectangular representation (I,Q) to polar representation.

The polar limiter needs to perform the following calculations:

- Calculate $A = I^2 + Q^2$

[1] In IEEE 802.11a/g

- Calculate $\Phi = \arg(I, Q)$, LUT/cordic
- Limit A
- Limit Φ
- Calculate $(I, iQ) = \sqrt{A}e^{i\Phi}$

This algorithm is very processing-power consuming if it is implemented in a general purpose DSP without support for polar-to-cartesian conversion and limit functions in hardware.

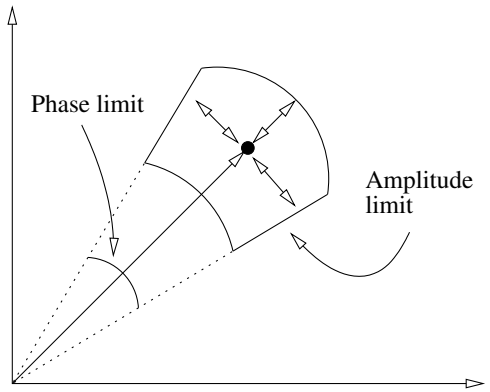

Figure 3: Polar limiter.

4 Proposed method

In this paper a similar solution is proposed. However, this solution is based on a *cartesian limiter* instead. The cartesian limiter limits the real and imaginary part independently of each other. This simple change simplifies the algorithm tremendously since there is no need to perform costly polar/cartesian and cartesian/polar conversions. However, the "cost" for this simplification is a slight increase in phase errors since cartesian limiters are more prone to change the phase of the limited signal.

The output from the cartesian limiter is:

$$X = \begin{cases} X & X' - \delta < X < X' + \delta \\ X' - \delta & X < X' - \delta \\ X' + \delta & X > X' + \delta \end{cases}$$

Where X is the input (I or Q) and X' the desired constellation point, δ is the maximum deviation from the desired constellation point.

However, limiting a a complex valued vector in a programmable DSP is an cycle consuming task which requires at least 8 instructions per complex sample if predicates can be used.

Since non-constant envelope modulation and constellation mapping to BPSK, QPSK, 16QAM, 64QAM are not limited to IEEE 802.11a or HiperLan/2, a variable saturation instruction for signal limiting is justified in conjunction with instruction level acceleration for FFT in a converged baseband solution for software defined radio, SDR.

By using a decimation in time (DIT), Radix-4 FFT for the inverse FFT and then using a decimation in frequency (DIF) FFT for the forward transform; 160 butterfly operations can be saved. They do not need to be calculated since we zero-pad the last 192 samples of the input data (interpolation), and then throw away the last 192 output samples (decimation).

One possible implementation of a limiter is shown in Figure 4. In order to create a complex cartesian limiter, the hardware in Figure 4 is doubled. This unit can integrated together in the MAC/R4-Butterfly by adding one extra stage of pipeline registers.

Depending on the memory architecture, the limiter can work transparent of the FFT operations, if the memory bandwidth is high enough to supply the previously calculated constellation points from the memory.

Another possibility to releave the memory interface is to include the limiter as a vector operation instruction in conjunction with a loop instruction.

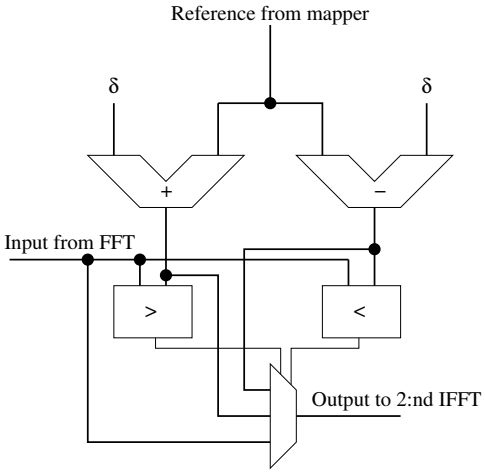

Figure 4: Real-valued limiter.

5 Results

Since the soft limiter based on cartesian limits is the most promising algorithm for implementation in a programmable DSP extensive simulations on "real" data from an IEEE 802.11a transmitter has been

carried out. Preliminary simulations have shown acceptable performance as shown below.

In the following table, the SNR is compared for different peak limits of real IEEE 802.11a data containing random bits. δ has been chosen to 0.15 for the cartesian limiter and a corresponding (A = 0.21, $\phi = 9°$) has been chosen for the polar limiter.

Limit	Polar	Cartesian
12 dB	-	-
9 dB	-	31.1 dB
6 dB	29.4 dB	24.2 dB
3 dB	22.1 dB	19.3 dB

The peak reduction performance is also compared for a 64 sample IEEE 802.11a symbol which had initial PAR of $\sim$ 12 dB.

Limit	Polar	Cartesian
9 dB	24.6 dB	24.4 dB
6 dB	20.2 dB	14.9 dB
3 dB	17.5 dB	13.8 dB

Furthermore, the computational cost is analyzed for phase and amplitude limiter and for the complete algorithm. In the following table, the cycle-cost for the phase and amplitude correction step of one sample is presented.

Task	Polar Limit	Cartesian Limit
$A = I^2 + Q^2$	3 cc	-
$\Phi = \arg(I, Q)$	72/48* cc	-
Limit point	8 cc	8 cc
$(I, iQ) = \sqrt{A}e^{i\Phi}$	72/48* cc	-
	155/107 cc	8 cc

*Using Coordic/LUT

The following table shows the cycle cost for the complete algorithm, assuming the FFT/IFFT is implemented by using a Radix-4 butterfly instruction.

Task	Cycle cost
IFFT (4 $\uparrow$)	112 cc
256 p. power limit	384 cc
FFT (4 $\downarrow$)	112 cc
Cartesian limit	512 cc
	1120 cc

The total cycle cost is $\sim$1250 clock cycles including control flow instructions. This corresponds to $\sim$320 Mop/s if the algorithm is run sequentially.

6 Future work

In order to further improve the peak to average reduction capability of the algorithm and reduce peak regrowth, several passes of the algorithm may be needed. This issue and further optimizations of the proposed algorithm will be investigated in the near future.

7 Conclusion

If only BER and PAR are considered, the soft clipping method using polar limits is the best choice to reduce PAR without significantly degrading BER. However, this method is very processing power intensive and has only a small advantage over cartesian limitation which is less computation intensive. Both algorithms benefit from a limit accelerator which both removes the data dependency in the program flow and improves performance by removing instruction and addressing overhead.

Preliminary simulation results on a IEEE 802.11a model verifies the peak reduction effect of soft clipping, using a cartesian limiter while only consuming a fraction of the computing power and only a minor SNR degradation compared to existing methods.

References

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