System Architecture for 3GPP LTE Modem using a Programmable Baseband Processor

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***Abstract*—3G evolution towards HSPA and LTE is ongoing which will substantially increase the throughput with higher spectral efficiency. This paper presents the system architecture of an LTE modem based on a programmable baseband processor. The architecture includes a baseband processor that handles processing such as time and frequency synchronization, IFFT/FFT (up to 2048-p), channel estimation and subcarrier demapping. The throughput and latency requirements of a Category 4 User Equipment (CAT4 UE) is met by adding a MIMO symbol detector and a parallel Turbo decoder supporting H-ARQ. This brings both low silicon cost and enough flexibility to support other wireless standards. The complexity demonstrated by the modem shows the practicality and advantage of using programmable baseband processors for a single-chip LTE solution.**

I. Introduction

3GPP Long-Term Evolution (LTE) is the 4th generation radio access technology which incorporates Orthogonal Frequency Division Multiple Access (OFDMA) as the multiple-access scheme in downlink. The downlink receiver chain of an LTE modem is depicted in Fig. 1.

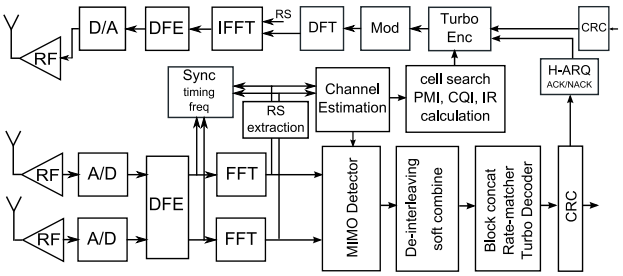

Fig. 1: Functional Flow of an LTE Modem (PHY only)

There are a number of design challenges for LTE such as frequency synchronization, channel estimation, MIMO detection, Hybrid Automatic Repeat ReQuest (H-ARQ) and high-throughput forward error correction (FEC) decoding. Meanwhile, in order to cover legacy standards (e.g. WCDMA/HSDPA and DVB) and other new standards (e.g. WiMAX), either multiple ASIC modems (one for each standard) have to be integrated into a chip or a programmable hardware which can handle multiple standards [1] has to be used. The first solution not only consumes a significant amount of hardware, it is also requires more integration work. The second solution is called software-defined radio (SDR) which exploits the similarity among different signal processing tasks to allow hardware multiplexing. SDR with an efficient architecture only consumes slightly more hardware while being able to support multiple standards, compared to single-standard ASIC solutions.

In [2], implementation issues of an LTE modem is presented with insight to both the algorithms and their implementation cost estimation. However, to the best knowledge of the authors, detailed information of SDR based LTE modems is not yet available in literatures. In this paper:

- The architecture and implementation results of an LTE category 4 modem based on a novel programmable baseband processor, LeoCore [1], is presented, which is the first SDR based LTE modem presented in the literature with architectural and performance information.
- The implementation of a MIMO detector that supports both MMSE and a novel low-complexity close-ML MIMO detection methods is presented.
- The implementation of a multi-standard parallel Radix-4 Turbo decoder that support both binary and duo-binary Turbo decoding is presented.
- The link-level performance of the complete LTE receiver is presented with various signal distortions taken into consideration. The degradation due to errors introduced in different processing stages is presented in the simulation result.

The remainder of the paper is organized as follows. In Sec. II, important features of an LTE modem are briefly reviewed. The system architecture and functional flow of an LTE receiver is presented in Sec. III. Sec. IV presents the architecture of the programmable baseband processor. The MIMO detector and the FEC processor that handles H-ARQ and Turbo decoding are presented in Sec. V. Sec. VI and VII present the simulation performance and area cost. Finally, Sec. IX concludes the paper.

II. Overview of 3GPP LTE Features

The LTE modem presented in this paper meets the physical layer requirements listed in Tab. I.

A. OFDMA and SC-FDMA

Being significantly different from 3GPP WCDMA/HSPA standards which uses code division multiple access (CDMA), LTE adopted OFDMA as the downlink access scheme and single-carrier Frequency division multiple access (SC-FDMA) as the uplink transmission scheme. The major difference

UE Category (CAT)	1	2	3	4
Supported Bandwidths	1.4, 3, 5, 10, 15, 20 *MHz*			
Antenna Configurations	up to 2x2 SM and SFBC			
Num of Layers for SM	1	2		
Max num of Soft-bits	250368	1237248	1237248	1827072
DL peak rate (Mbit/s)	10	50	100	150
UL peak rate (Mbit/s)	5	25	50	50

TABLE I: Supported LTE UE Categories

between OFDMA and SC-FDMA is that the latter introduces one extra Discrete Fourier Transform to mitigate the peak-to-average power ratio problem.

B. Multi-Antenna

Multi-antenna (MIMO) technologies have been incorporated into LTE. As defined in [9], spatial multiplexing (SM) and transmit diversity (space-frequency block coding, SFBC) are the two MIMO schemes used in different scenarios. As depicted in Fig. 2, the antenna mapping consists of two parts namely layer mapping and precoding. The former multiplexes the modulated symbols belonging to one or two codewords into different number of layers (or codeblocks) to transmit. The latter loads symbols from each layer and maps them to different antennas and subcarriers. Only two antennas are considered by UE CAT1-4. In OFDMA systems such as LTE, the general transmission model of each subcarrier is

$$r = \mathbf{H}s + n \tag{1}$$

where $\mathbf{H}$ is the frequency domain channel matrix, s and r are in respect the transmitted and received symbol vector.

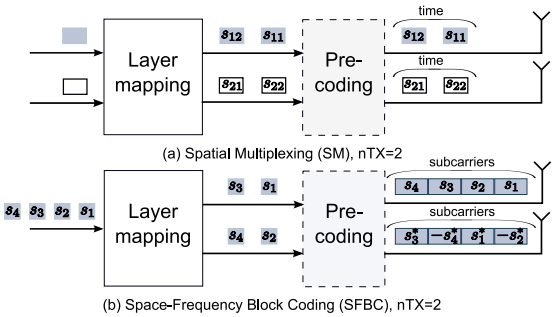

Fig. 2: Downlink Multi-antenna Transmission Schemes

III. System Architecture

The processing flow of an LTE physical downlink shared-channel (PDSCH) which is the major part of a LTE receiver is illustrated in Fig. 1. Note the modem implementation presented in this paper only includes the physical layer assuming higher layers (e.g. RLC and MAC) are handled by a microcontroller (e.g. ARM-Cortex8). The key modules in the flow are presented in the following sections.

A. Digital Front-End (DFE)

The DFE unit is the bridge between the Analog Front-End (AFE) and Digital BaseBand (DBB) part in the wireless systems. The function of DFE is usually gain control, sample rate conversion, pulse shaping, matched filtering and sometimes phase adjustment. Generally speaking, it is mainly a block of digital filters. Although from a functionality perspective the DFE is rather simple compared to other baseband blocks which diversify according to various standards, it still consumes a significant portion of the die area and power. A configurable DFE which supports multiple standards is included in the baseband processor.

B. Synchronization

Being an OFDM system, LTE is sensitive to Carrier Frequency Offset (CFO) which causes inter-carrier interference. By utilizing the method in [4], timing synchronization and fractional CFO estimation can be performed. Integer frequency offset estimation is then applied to remove misalignment which is integer multiple of the subcarrier spacing. Thereafter, even though most of the CFO has already been compensated for, there is still a Residual Frequency Offset (RFO) due to estimation errors. RFO is estimated based on the frequency-domain symbols after FFT.

C. Channel Estimation

Like many other OFDM system (e.g. DVB-H), pilot symbols (which is called reference signals in LTE) are inserted during subcarrier mapping in both time and frequency directions. The major difference here is the use of multiple antennas. Being different from the typical "MIMO-OFDM" channel estimation problems [3] in academia, the reference signals transmitted from multiple antennas are orthogonal to each other which means the channel impulse response between different Tx-Rx antenna pairs can be separately estimated. This avoids the high complexity of real "MIMO" channel estimation at the cost of lower spectrum efficiency due to the "silent" subcarriers carrying nothing.

D. Detection

For MIMO systems, a major challenge is the separation and detection of the transmitted symbols at the receiver [5]. Due to the amount of operations involved, such as matrix inversion, it cannot be handled by the baseband processor itself. Among different detection algorithm, Maximum Likelihood (ML) detection is an optimum detector that computes

$$L(b_i|r) = \log\left(\frac{\sum_{s:b_i(s)=1}\exp(-\frac{1}{N_o}\|r-\mathbf{H}s\|^2)}{\sum_{s:b_i(s)=0}\exp(-\frac{1}{N_o}\|r-\mathbf{H}s\|^2)}\right) \tag{2}$$

Here "$s : b_i(s) = \beta$" means all s for which the ith bit of s is equal to β. Computing (2) requires enumeration of the entire set of possible transmitted vectors. The complexity of doing this is usually not affordable for implementation in practice. However since ML provides the best theoretical performance, it is commonly used as a benchmark when comparing other algorithms. Linear detection such as Minimum Mean-Square-Error (MMSE) has very low complexity. MMSE detection is defined as follows

$$MMSE : \hat{s}_{MMSE} = (\mathbf{H^H H} + \sigma^2\mathbf{I})^{-1}\mathbf{H}^H r \tag{3}$$

Being the most widely used detection scheme, MMSE detection involves matrix inversion which can be efficiently handled through direct inversion with sufficient numerical stability [13]. Despite the low complexity, MMSE detection has relatively poor performance especially when the channel is slow-fading [5]. As a trade-off between detection performance and implementation complexity, close-ML soft-output detectors such as [5] and [6] can be used. In [5], a fixed complexity close-ML detector is presented which substantially reduces the complexity by only partially enumerating the symbols selected for exact marginalization. More importantly, it has a fully parallel structure which makes it suitable for parallel implementation. Hence it is chosen for this implementation.

E. FEC and H-ARQ

In order to provide reliability as well as mobility of the data transmission over radio channels, Forward-Error Correction (FEC) codes such as Turbo code and Convolution code are used in LTE. These add redundant information before transmitting the data, and they are indispensable to achieve robust data transmission. Meanwhile, H-ARQ is used together with FEC to improve the throughput by retransmitting corrupted packets. Similar to WiMAX, two soft-combining methods namely Chase Combining (CC) and Incremental Redundancy (IR) are used to combine the LLR of a retransmitted packet with its previously received copies. In CC, the basestation retransmits the same packet when it receives the NACK signal from UE, and UE combines the LLR information generated by the detector with those of the initially received packet. While in IR, each retransmission carries a new set of parity bits to be combined with the initially received systematic and a few parity bits. Since the amount of operations involved in Turbo decoding is significant, it has always been the bottleneck of the baseband processing which is latency constrained. Meanwhile, H-ARQ requires a large soft buffer in proportion to the data rate. The soft-buffer sizes of different UE categories are defined in Tab. I. Both the Viterbi and CRC decoders are also implemented as accelerators attached to the processor.

F. Others

Other things such as cell search and the computation of Precoding Matrix Indication (PMI) and Channel Quality Indication (CQI) at the UE side also involve significant amount of operations. These are handled by the baseband processor.

G. Functional Mapping

The radio signals received by the radio frequency front-end will be downconverted to analog baseband signals, then converted to digital baseband signals by the analog-to-digital converters (A/D). The digital front-end (DFE) applies filtering to the baseband signals and FFT is applied to convert the time-domain signal into frequency-domain where channel estimation and symbol detection occur. In LTE, the channel estimator will use the reference signals (RS) to estimated the MIMO channel matrices $\mathbf{H}$ for all data subcarriers. The estimated $\mathbf{H}$ and received symbol vector r belonging to the current user will be extracted for MIMO detection later. All the work above is handled by the baseband processor. The cycle cost of tasks (for 20 MHz bandwidth, 2×2 SM) mapped on LeoCore is presented in Tab.II.

Then, $\mathbf{H}$ matrices will be passed to the MIMO detector together with the received symbols extracted from data subcarriers. The coefficients will be fed to the detector to compute the LLR soft-output $L(b_i^k)$. For example, in case of MMSE detection is used, the detector loads W from the memory and multiplies W with the received symbol vectors r to compute $\hat{s}$ and to demap $\hat{s}$ to LLR values. The LLR values will be passed to the Forward-Error-Correction (FEC) part where it will be de-interleaved and processed by the channel decoder to generate the final hard-decision of the transmitted bits. The FEC part mainly contains the soft-buffer for Chase Combining in H-ARQ and a parallel Turbo decoder which delivers a high throughput which is more than 170 Mbit/s.

Function	Million Cycles/Second
Timing & Frac Freq Sync	8
Integer Freq Sync	12
Residual Freq Sync	18
FFT	88
Channel estimation	80
PMI & CQI & RI Calculation	40

TABLE II: Cycle Cost of UE Receiver

IV. BASEBAND PROCESSOR

The LTE modem is based on a programmable baseband processor targeting multi-standard radio baseband processing [1]. It adopted a novel architecture namely Single Instruction Multiple Tasking (SIMT) and an architecture overview is presented in Fig. 3.

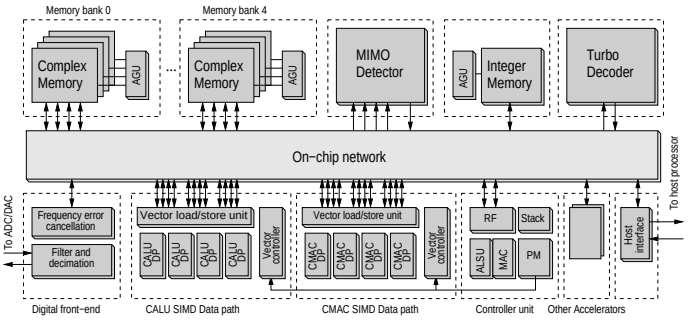

Fig. 3: Baseband Processor Architecture Overview

A. SIMT Architecture

The major components in the SIMT architecture are: SIMD vector execution units, memory banks, the on-chip network, accelerators and an integer controller core. The SIMT processor uses vector instructions that operate on large datasets in SIMD execution units. The key idea in the SIMT architecture is to issue only one instruction each clock cycle but still allow several operations to execute in parallel since vector instructions may run for several clock cycles on the SIMD units. This approach results in a degree of parallelism

equivalent to a VLIW processor without the need for the large control-path overhead.

In this way the fact that modem processing to a large extent consists of operations on large vectors of data, is used to get a processor with high utilization of execution units and low control overhead. For example the integer data-path could execute control tasks while the CMAC performs one layer of an FFT and the CALU performs pilot tone extraction.

To be able to take full advantage of the SIMT architecture, several key architecture components are necessary: efficient vector execution units, a matching memory system and a controller core capable of managing several threads efficiently. The SIMT architecture utilizes multiple complex valued SIMD execution clusters such as complex MACs and complex ALUs. Programmable co-processors and accelerators, in this case the MIMO detector and the Turbo decoder, can also be attached to the on-chip network and be seamlessly integrated in the processor architecture.

The processor is controlled by the controller core, which includes the program memory, instruction issue logic and functions for multi-context support. The controller core executes all control flow functions as well as integer based instructions.

B. Memory system and On-chip network

To enable several concurrent vector operations, a distributed memory system is used where the memory is divided into several memory banks, with individual address generation units (AGU). This arrangement in conjunction with the on-chip network improves the power efficiency of the memory system. This also increases the throughput of the processor as multiple address calculations can be performed in parallel.

The on-chip network is realized as a restricted crossbar switch which is under direct software control. Hence no arbitration is necessary and the performance is fully predictable. This allows software tools to use static scheduling of both network transactions as well as for vector instructions.

Co-processors attached to the on-chip network can utilize the same addressing modes as the vector instructions. In this way OFDMA pilot extraction can be done in parallel with MIMO symbol detection and channel estimation.

The memory system in the SIMT processor instance used in this paper has a memory bandwidth of 1024 bits per clock cycle for the complex valued memory system and 80 bits per clock cycle for the integer memory system.

V. Configurable Accelerators

Although many baseband processing tasks can be mapped to the programmable processor mentioned in Sec. IV, there are still a few tasks which need to be implemented in dedicated hardware to meet the performance and power constraints. For the UE category 4 requirement, two accelerators are added to the on-chip network. They are controlled by a number of control registers which can be set by the baseband processor.

A. MIMO Symbol Detectors

As presented in Sec. III, MIMO detection is one the of most performance demanding tasks in the receiver. There is a gap between linear detectors (e.g. MMSE) and close-ML detectors (e.g. MFCSO [5]) with respect to performance and implementation cost. In order to allow different MIMO detection algorithms to be incorporated into the same hardware, both an MMSE MIMO detector and a combined MMSE/MFCSO MIMO detector have been designed for the modem. As presented in the [7], the former one supports only MMSE detection based on the method presented in [13] for 2×2 SM and up to 64-QAM modulation schemes. Implemented using using ST 65nm CMOS process, it only consumes $0.14\ mm^2$ area. In comparison, the combined detector supports real-time MFCSO detection for 2×2 SM and up to 64-QAM modulation schemes. As presented in [7], an MFCSO detector contains an MMSE detector and since the MMSE mode will consume substantially lower power than the MFCSO mode, the detector is switched to MMSE mode when the UE enters power-saving mode. The combined dual mode MMSE/MFCSO detector consumes less than $0.3\ mm^2$ area which is only 2 times that of the MMSE-only detector. Running at 200 MHz clock, both detectors can support real-time detection of full 20 MHz band. For low-end modems which focuses on connectivity with minimum cost (e.g. smartphones), the MMSE-only detector can be integrated. For high-end modems, where performance is the key issue, the dual mode MIMO detector should be integrated. Both detectors support the detection of all MIMO schemes defined in LTE. The block diagram of the dual mode detector is depicted in Fig. 4. The channel preprocessor handles channel-rate processing tasks (e.g. the inversion of the channel matrices $\mathbf{H}$) which is done once the estimated channel is updated. The computed coefficient matrices W will be stored in the coefficient buffer and fed to the LLR demapper as input. The LLR demapper computes the LLR values using the MFCSO method presented in [5]

$$L(b_k^i) = -\frac{1}{\sigma^2}\Big\{ \min_{\mathbf{l}\in\mathcal{L}_\mathbf{k}:\mathbf{b}_\mathbf{k}^\mathbf{i}=\mathbf{0}} \delta - \min_{\mathbf{l}\in\mathcal{L}_\mathbf{k}:\mathbf{b}_\mathbf{k}^\mathbf{i}=\mathbf{1}} \delta \Big\} \tag{4}$$

The LLR demapper contains a number of processing elements (PE) which can utilize the parallelism in the algorithm. The computed LLR values $L(b_k^i)$ are stored in the soft-buffer for CC in H-ARQ.

B. Parallel Turbo Decoder

According to the definition of LTE parameters in Tab. I, up 150 Mbit/s peak data rate for downlink needs to be supported. With traditional Turbo decoder that contains a single SISO, the theoretical throughput is around 25Mbit/s. Hence a new parallel Turbo decoder is needed to supply higher data rates. Although Turbo decoders based on SIMD architectures [8] exist, they are not competitive compared to dedicated implementations. Furthermore, since the variation of Turbo decoding procedure among different standards is small, a configurable accelerator is sufficient to achieve enough flexibility while maintaining area and power efficiency. In

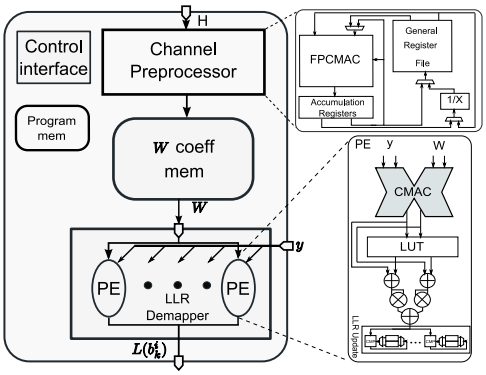

Fig. 4: Block Diagram of the Dual-mode MIMO Detector

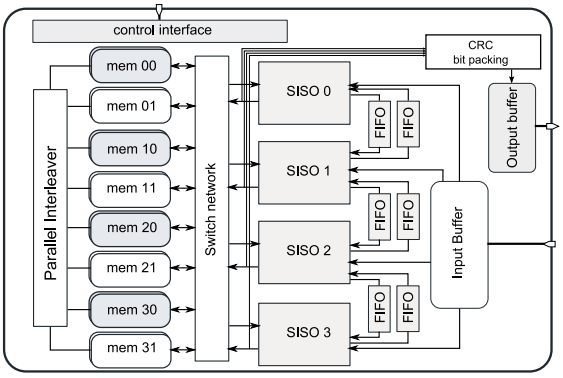

Fig. 5: Block Diagram of the Parallel Turbo Decoder

order to supply 150 Mbit/s peak data rate required by LTE UE category 4, a parallel Turbo decoder with four SISO units has been designed and it is depicted in Fig. 5. Each SISO unit supports Radix-4 log-Max decoding with the scaling of the extrinsic information by a factor ranging from 0.6 to 0.8. A sliding window technique is used inside the SISO decoder with a windows size of 64. Thanks to the QPP interleaver which allows conflict-free parallel access, the implementation of the parallel interleaver is based on the method presented in [14]. Synthesized using 65 nm CMOS process, the Turbo decoder easily runs at 300 MHz with a silicon area of $0.5\ mm^2$. The throughput of the Radix-4 decoder working in LTE mode is

$$T = \frac{S_{blk,max} \times f_{clk}}{(\frac{S_{blk,max}}{2 \times N_{siso}} + S_{window} + C_{extra}) \times 2 \times N_{ite}} \quad (5)$$

where $S_{blk,max} = 6144$ is the maximum number of bits per codeword defined in [10], $N_{siso} = 4$ is the number of SISO units, $S_{window} = 64$ is the sliding window size, $C_{extra} = 10$ is the number of overhead cycles, $f_{clk} = 300\ MHz$ is the clock frequency and N_{ite} is the number of decoding iterations. The throughput of the decoder is 137Mbit/s in case $N_{ite} = 8$. However, when SNR is relatively high, early stopping can effectively reduce the number of iterations needed to 4–6. This gives a throughput of 182–273 Mbit/s. Theoretically, for 20 MHz bandwidth with 2x2 SM and 64-QAM, the required throughput of Turbo decoding is 176 Mbit/s, which means the presented implementation is sufficient for CAT4 PDSCH decoding. Owing to the scalability of the on-chip network, the Turbo decoder is easily wrapped and integrated with the modem platform. Although the current FEC implementation only supports CC, it is straightforward to extend it to support IR. The maximum size of the soft-buffer is defined according to the UE category in Tab. I. The Turbo decoder is also designed to support the duo-binary convolutional Turbo decoding required in WiMAX (a self-tailing Radix-4 Turbo with different trellis). The WiMAX mode has a slightly higher latency (one extra window size), though it is still sufficient to support the highest data rate.

VI. Performance Analysis

In order to carry out both fast prototyping and verification of the 3GPP LTE modems, a complete physical layer simulation chain has been developed in Matlab and C. Combination with an LTE signal generator, it allows both quantitative performance evaluation and conformance testing of the chip. The simulation chain includes a transmitter conforming to 3GPP technical spec (e.g. [9][10]). The 3GPP SCME model [11] is used as the channel model. In the simulation done for this paper, 8000 subframes are simulated. To compared the performance of MFCSO and MMSE detection, 2×2 SM is used. No close-loop precoding is assumed in this paper. At most three retransmissions are allowed in CC based H-ARQ. The throughput figures are calculated based on the method in [12]. Simulation parameters are listed in the Tab. III.

CQI	14
Modulation and Coding	64-QAM, 6/7 Turbo
System bandwidth	5 MHz
Channel model	Urban Micro
UE speed	3km/h
Carrier frequency offset	39kHz
Channel estimation	Least Squares
H-ARQ	Chase Combining, 3 retr
Turbo iterations	8 max, early stopping

TABLE III: Simulation Parameters

In Fig. 6 and 7, simulation settings represented in acronyms such as EC (estimated channel), PC (perfect channel), CFO (with carrier frequency offset), RFOC (residual frequency offset cancellation), PT (parallel log-Max Turbo) and ST (serial log-Max Turbo). The result shows

- The degradation caused by approximation (e.g. parallel windowing and sliding windowing) introduced in the parallel Turbo decoder is rather small (1 Mbit/s difference in throughput) when compared with the serial log-Max Turbo decoder.
- Severe performance degradation incurs when the residual frequency offset is not corrected. When it is corrected by RFOC, the loss due to CFO is negligible in this implementation.
- The MFCSO detector substantially outperforms the MMSE detector (more than 50% higher throughput) in 2x2 SM.
- The least squares based channel estimation has limited performance which implies the need of more advanced channel estimation (e.g. cascaded Wiener filters).

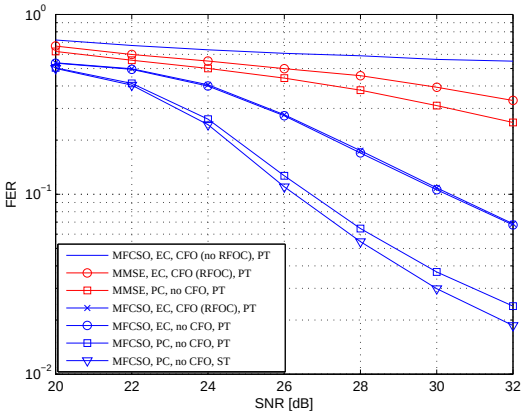

Fig. 6: Frame-Error-Ratio (2×2 SM, CQI=15, 5 MHz band)

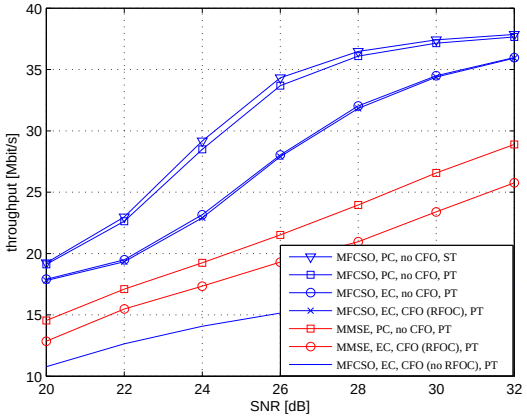

Fig. 7: Coded Throughput (2×2 SM, CQI=15, 5 MHz band)

VII. Area Analysis

Based on 65 nm CMOS technology, the baseband processor (including MIMO DFE, Viterbi decoder and Turbo Encoder etc.) consumes 270 kgates. Including the 1T-SRAM soft buffer defined in Tab. I, the pads and the pad rings, the total area of the CAT4 LTE modem (physical layer only) baseband chip is estimated to be $8\ mm^2$. When running at 250 MHz clock frequency, the processing capacity of PDSCH on the full 20 MHz band with 2×2 SM and 64-QAM modulation (which gives a data rate up to 120 Mbit/s at 28 dB) is supported.

VIII. Other Standards

As presented in [1], the baseband processor has been demonstrated to support real-time DVB-T/H receiving. It has also been proven to support mobile WiMAX by mapping the kernel parts of WiMAX baseband processing to it. With the aid of MIMO detector and the parallel Radix-4 Turbo decoder presented in this paper, a clock frequency of approximately 160 MHz allows an implementation of a Wave2 compliant mobile WiMAX terminal using 10 MHz channel bandwidth with 2x2 MIMO and H-ARQ.

IX. Conclusion

This paper presents the system architecture of a 3GPP LTE CAT4 modem which is based on a programmable baseband processor, a combined MMSE/MFCSO MIMO detector and a parallel Turbo decoder. The simulation results validates the baseband algorithms chosen to be implemented. The cost and performance analysis of the implementation shows that an SDR implementation of a commercial mobile broadband modem is feasible.

X. Acknowledgement

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